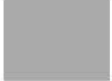


Apple 
Application Processor

Package Analysis Report

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Device Summary Sheet

Manufacturer: Apple Inc.
Part Number: 
Date Code: Not identified
IC Type: 64-bit quad-core SoC

Technology synopsis

Package Type: BGA
Pin Count: 1407
Package Size: 14,4 mm x 15,8 mm x 0,9 mm
Die Count: 3. One  processor die and two Micron LPDDR4 memory dice
 **Die Size:** 10,92 mm x 11,53 mm (by edge of physical silicon)
10,9 mm x 11,34 mm (by edge of seal)
Micron LPDDR4 Die Size: 12,88 mm x 6,92 mm (by edge of physical silicon)
12,82 mm x 6,86 mm (by edge of seal)
 **Die Thickness ¹ :** 162 µm
Micron LPDDR4 Die Thickness ¹: 108 µm
Processor Package Substrate Thickness ¹: 39 µm
Memory Package Substrate Thickness ¹: 87 µm

¹ Measured feature sizes are accurate within 2%

Source Device



Figure 1. Apple iPhone front side



Figure 2. Apple iPhone back side



Figure 3. Apple iPhone main PCB side A





Figure 4. Apple [redacted] iPhone [redacted] main PCB side B

Die and Package



Figure 5. Package top

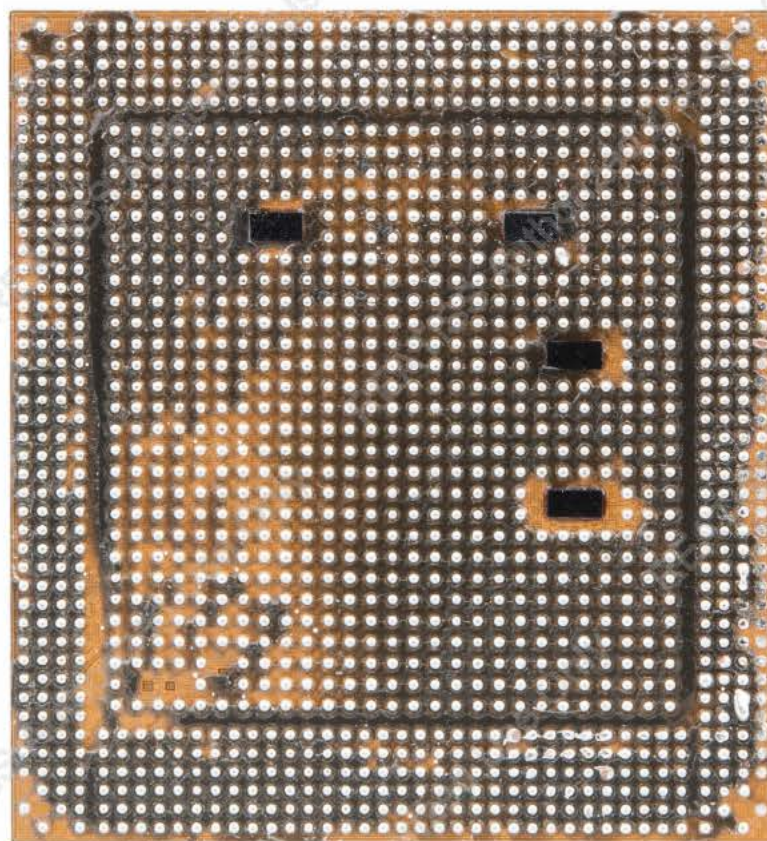


Figure 6. Package bottom

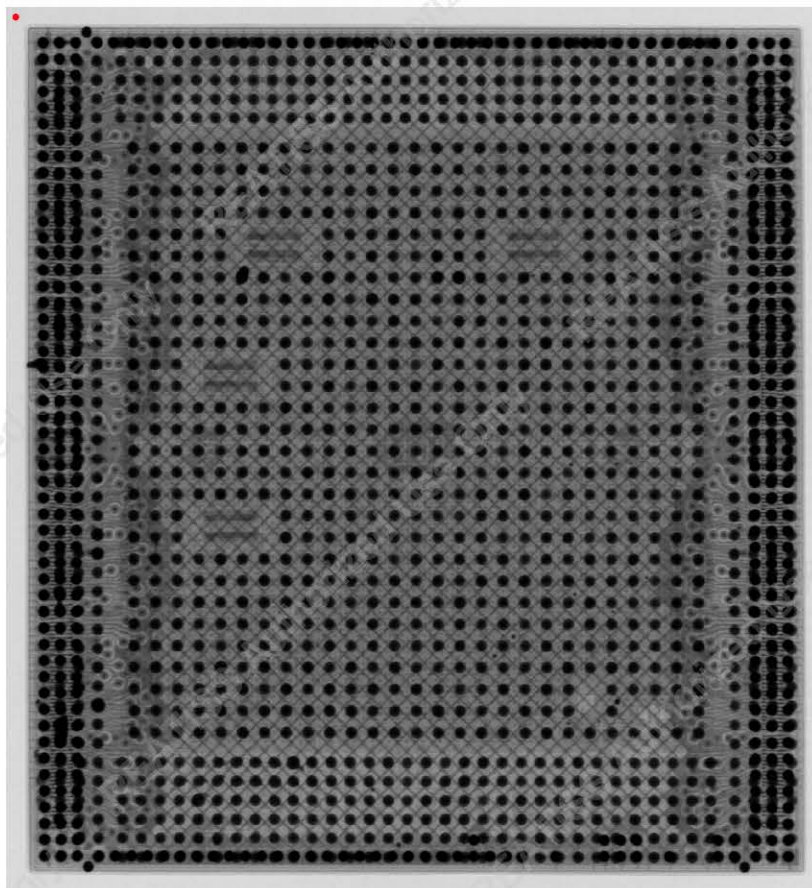


Figure 7. Package X-ray

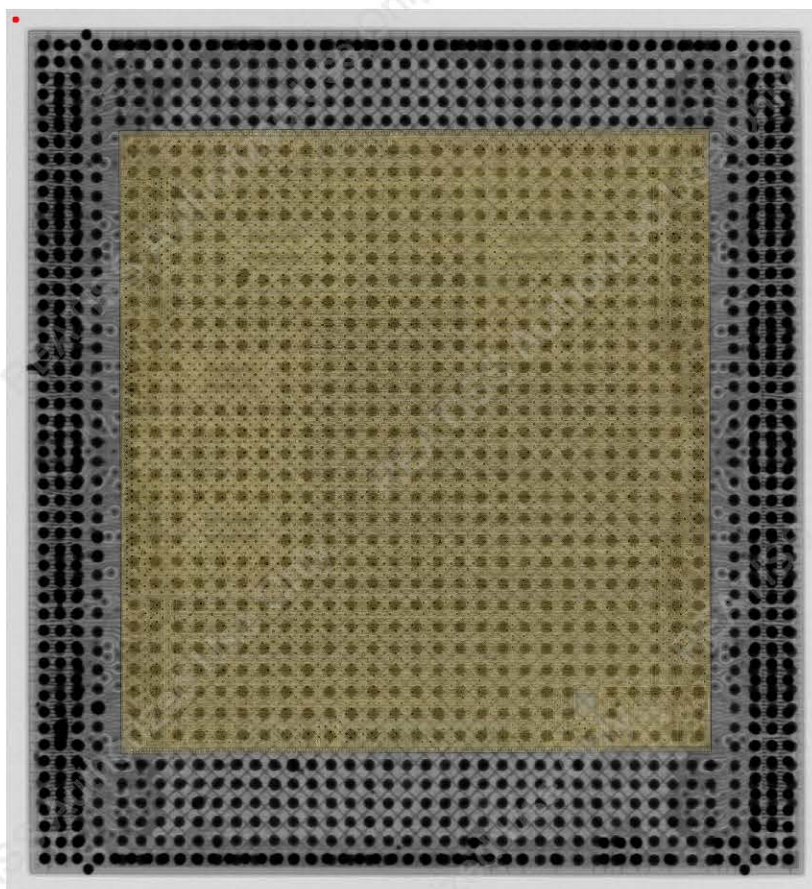


Figure 8. Package X-ray combined with  die photo

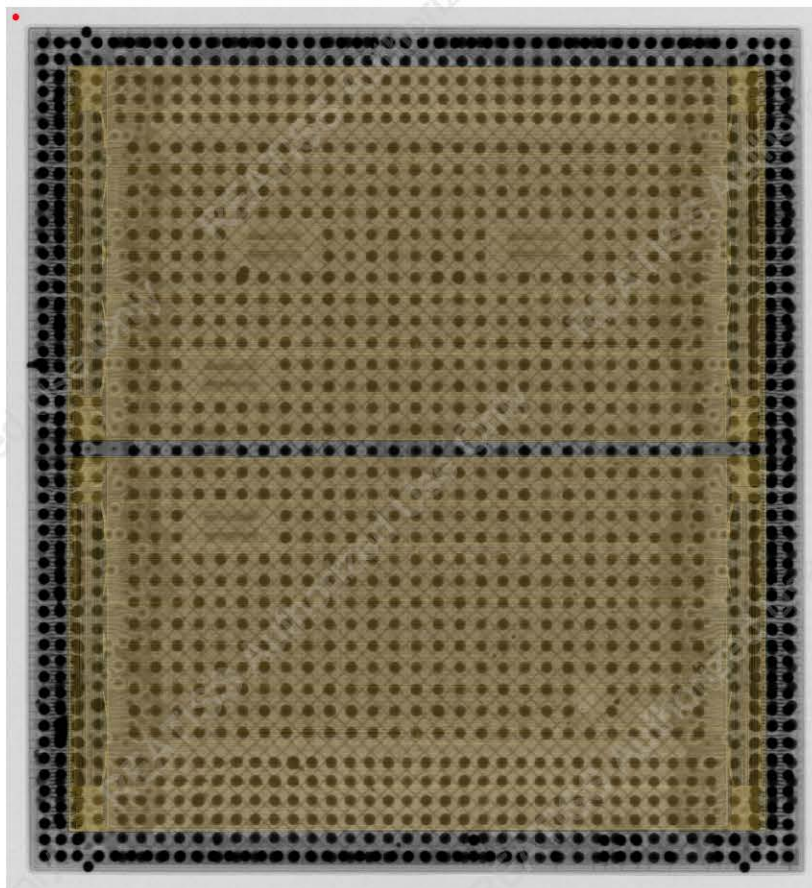


Figure 9. Package X-ray combined with Micron LPDDR4 dice photos

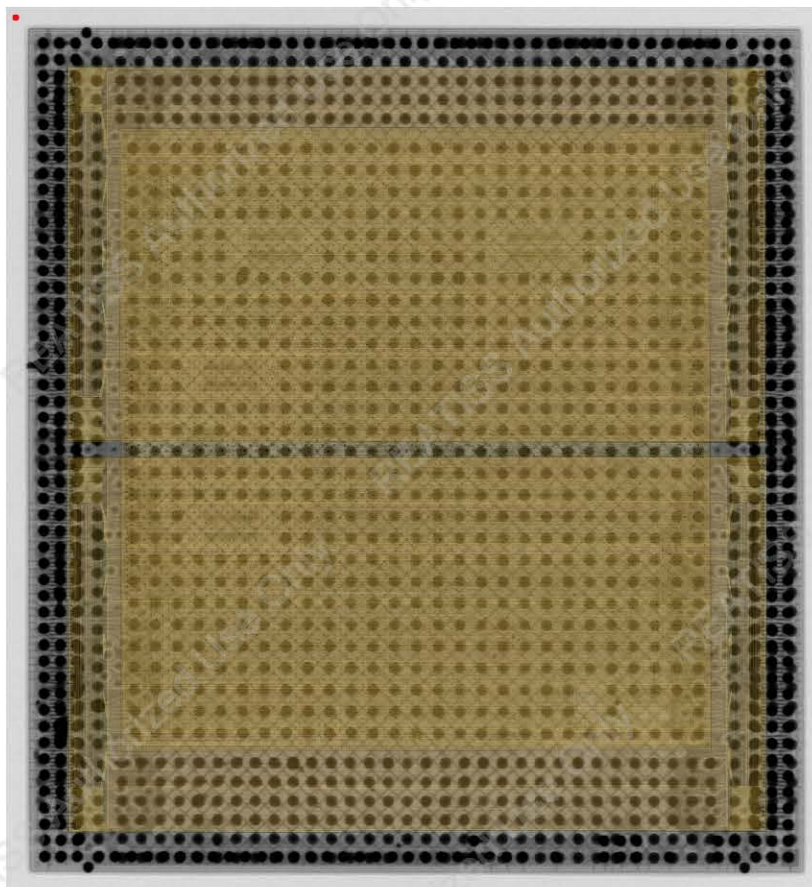


Figure 10. Package X-ray combined with dice photos



Figure 11.  die photo (top metal)



Figure 12.  die markings



Figure 13. Micron LPDDR4 die photo (top metal)



Figure 14. Micron LPDDR4 die markings

Package Analysis

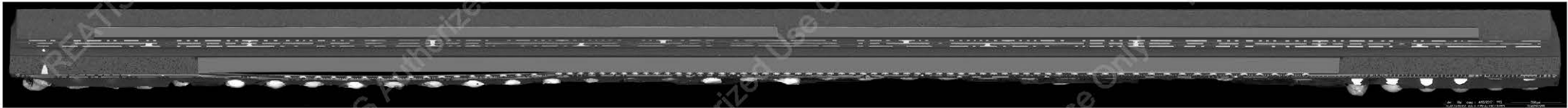


Figure 15. Package cross section

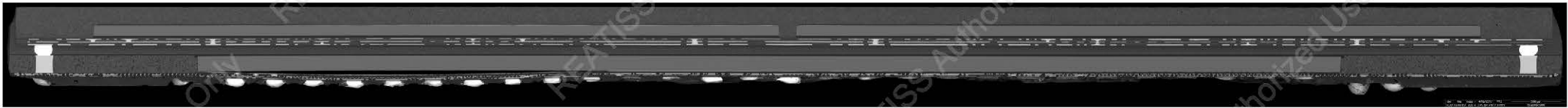


Figure 16. Package cross section (through package connection)

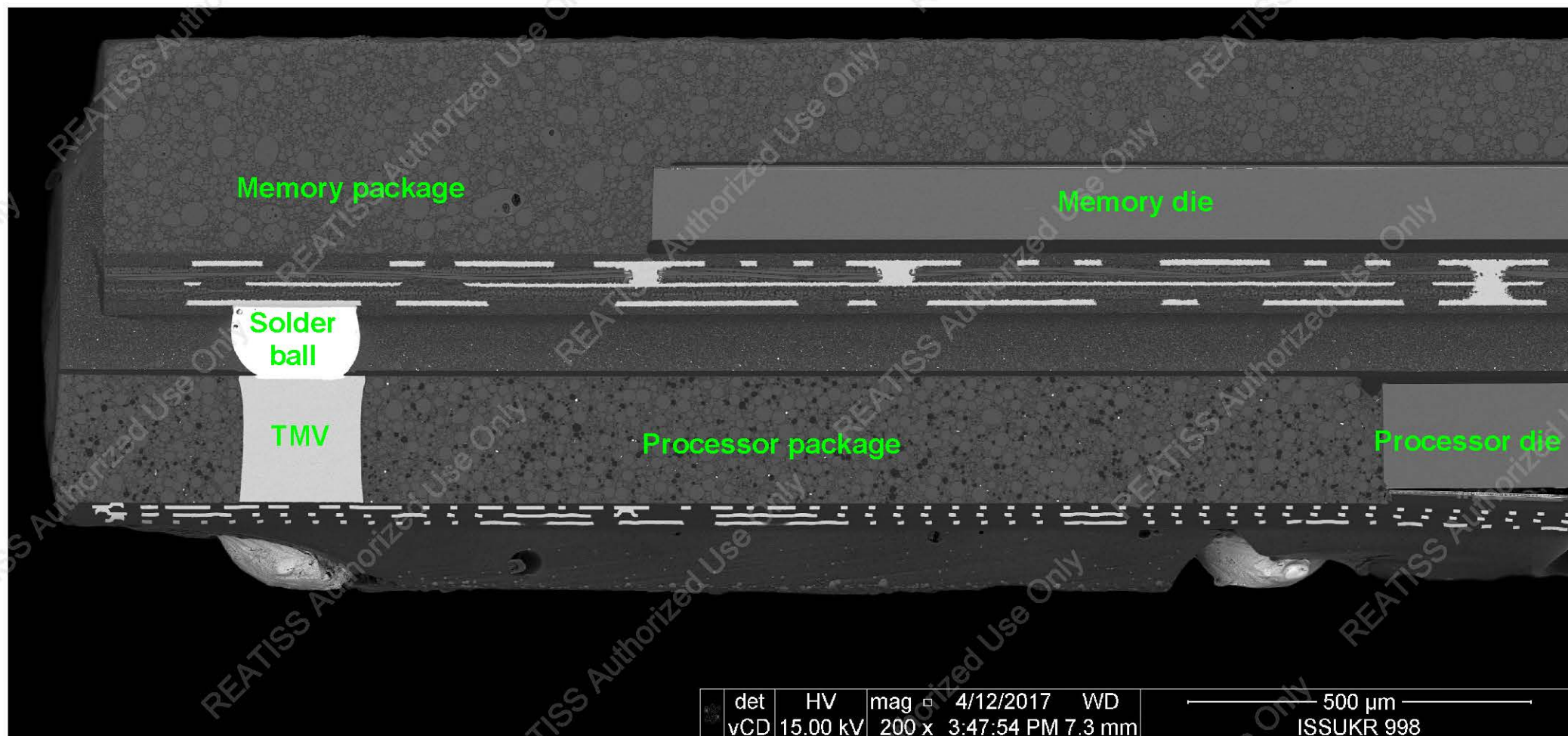


Figure 17. Package assembly left edge



Figure 18. Package assembly right edge

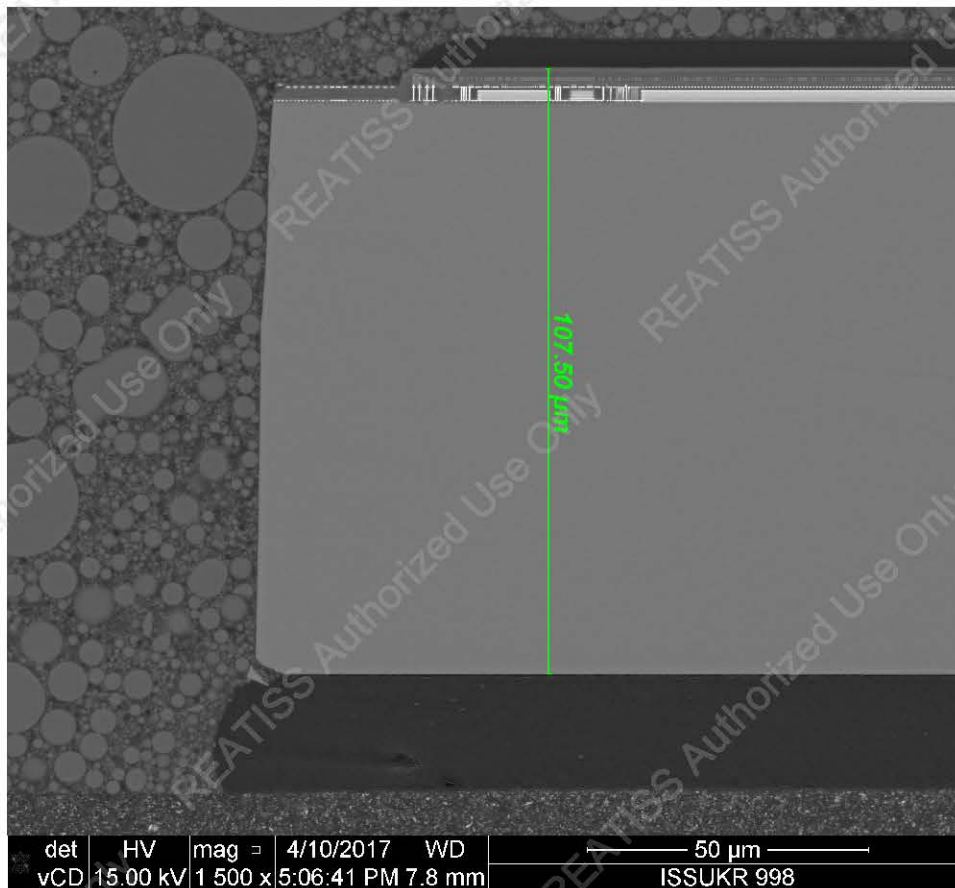


Figure 19. Memory die assembly

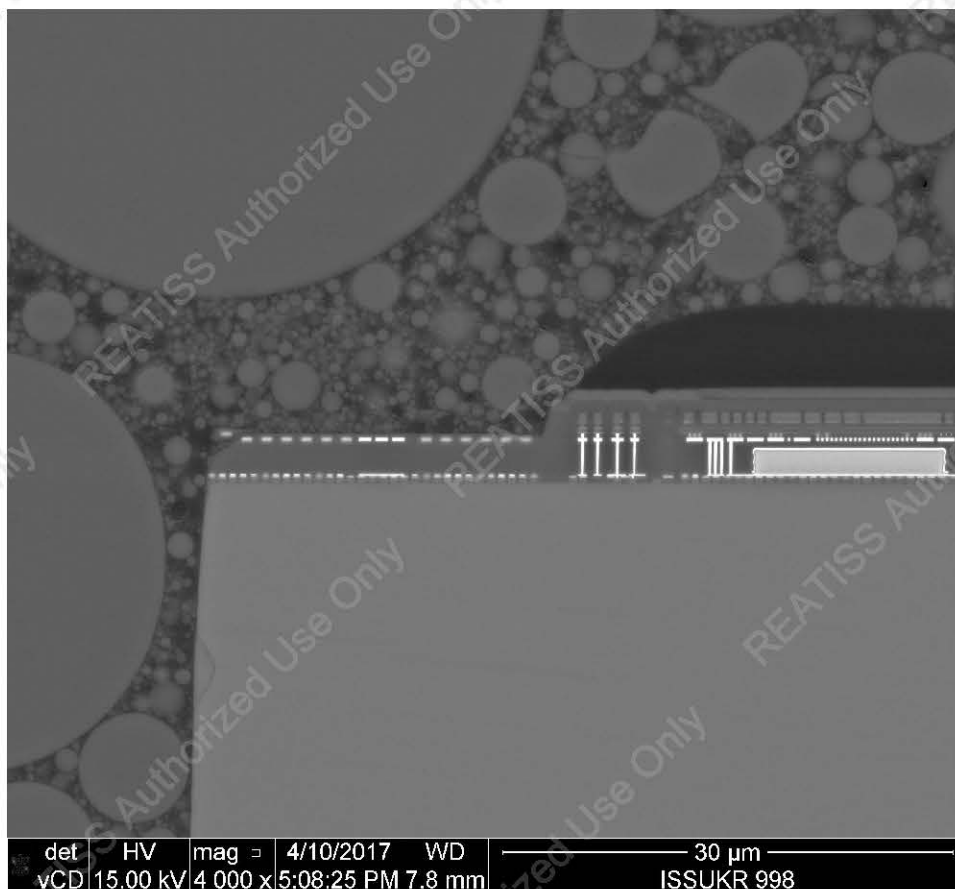


Figure 20. Memory die corner and encapsulation

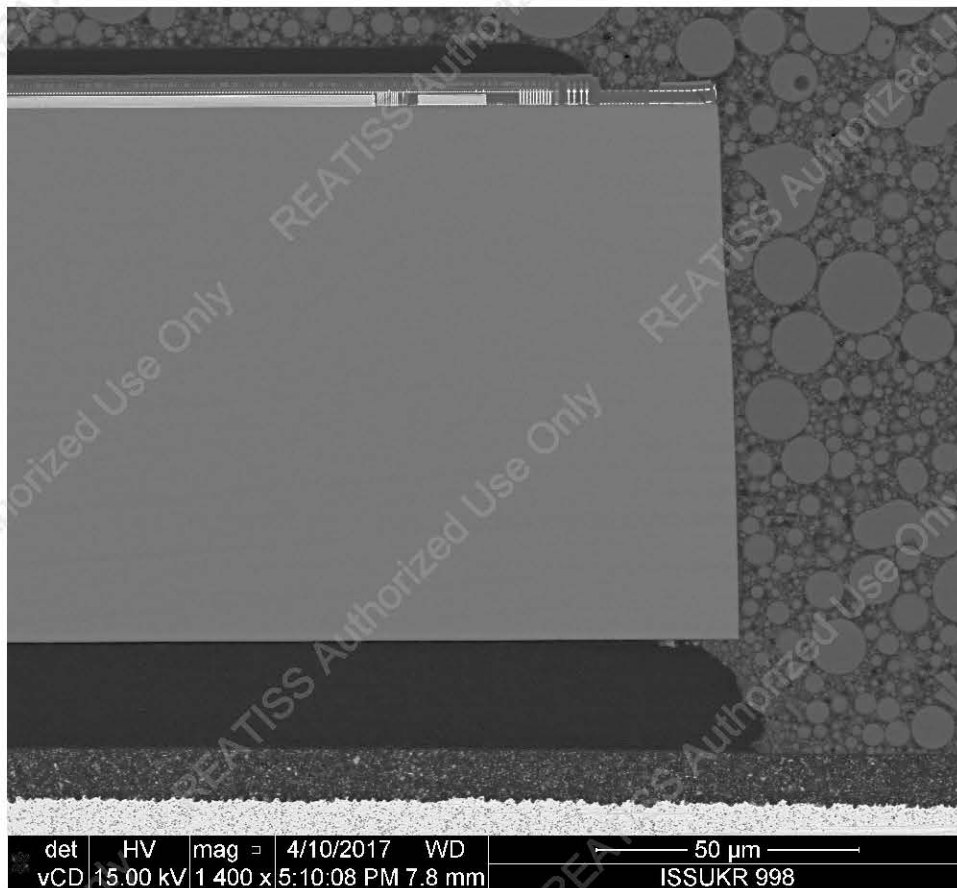


Figure 21. Memory die assembly

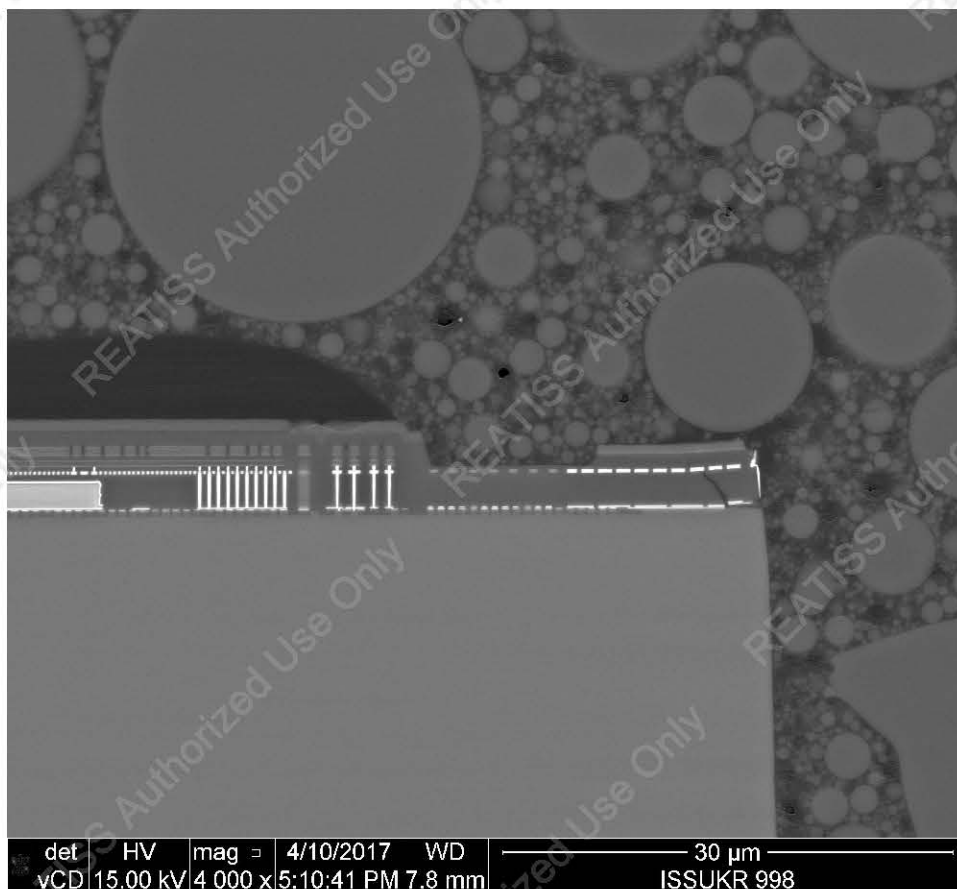


Figure 22. Memory die corner and encapsulation

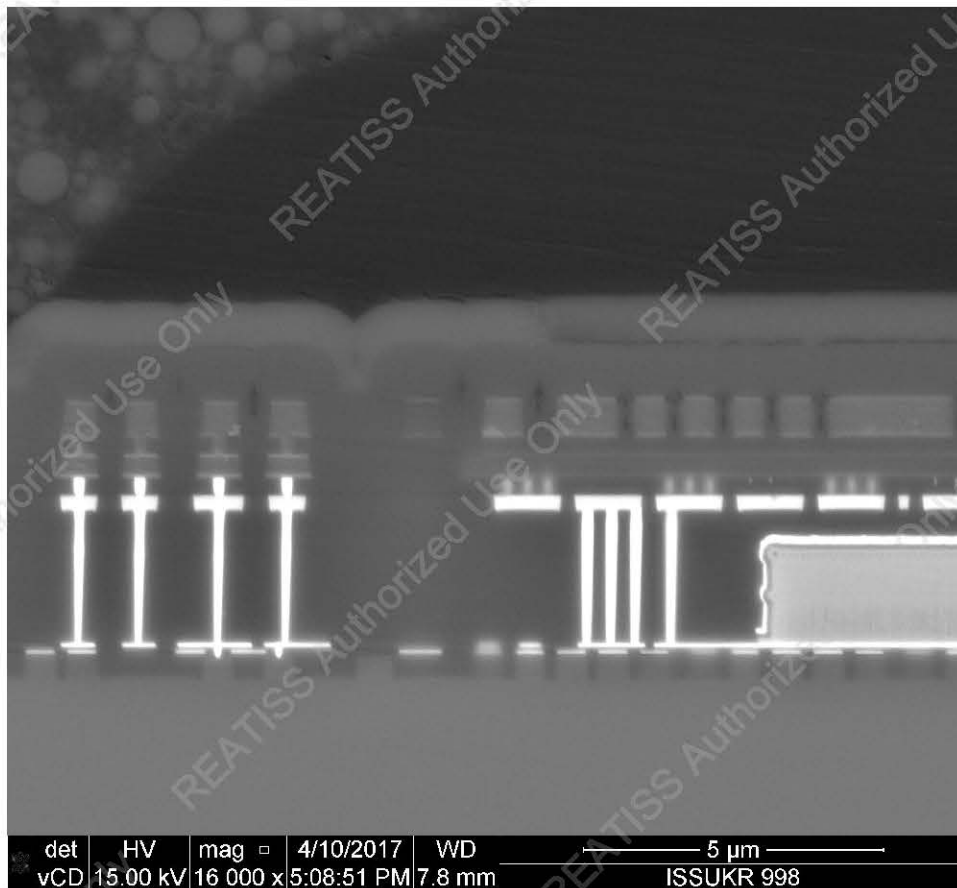


Figure 23. Memory die edge seal ring

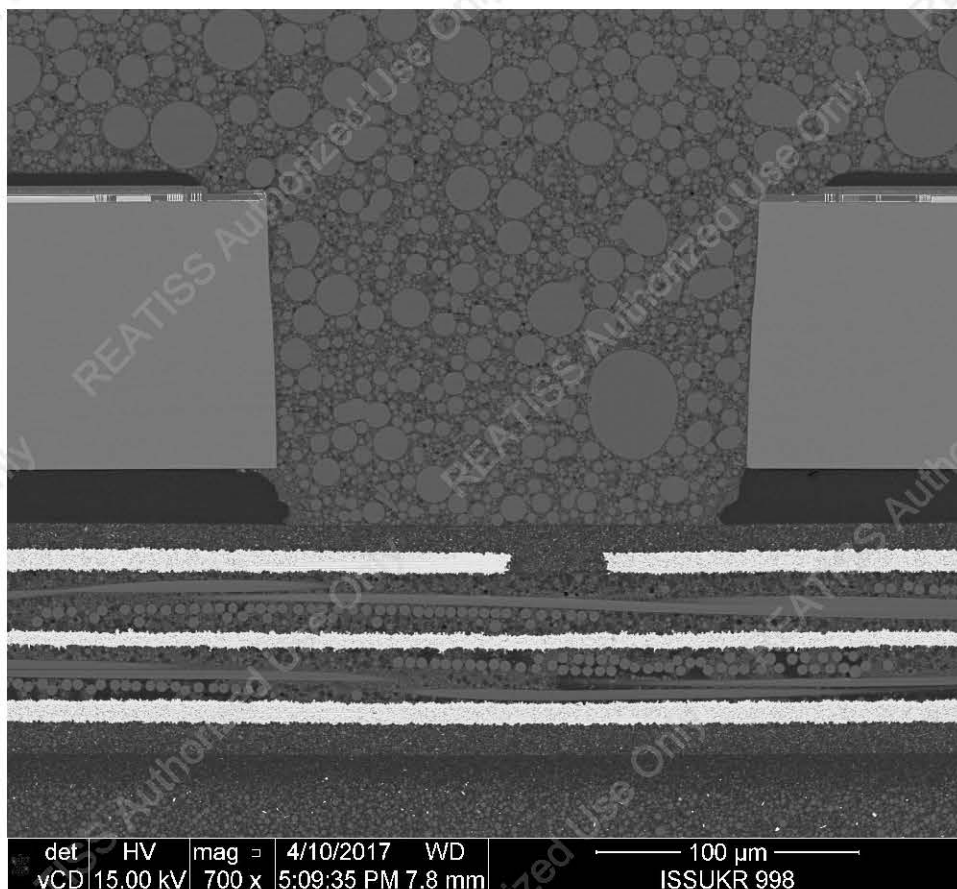


Figure 24. Memory dice

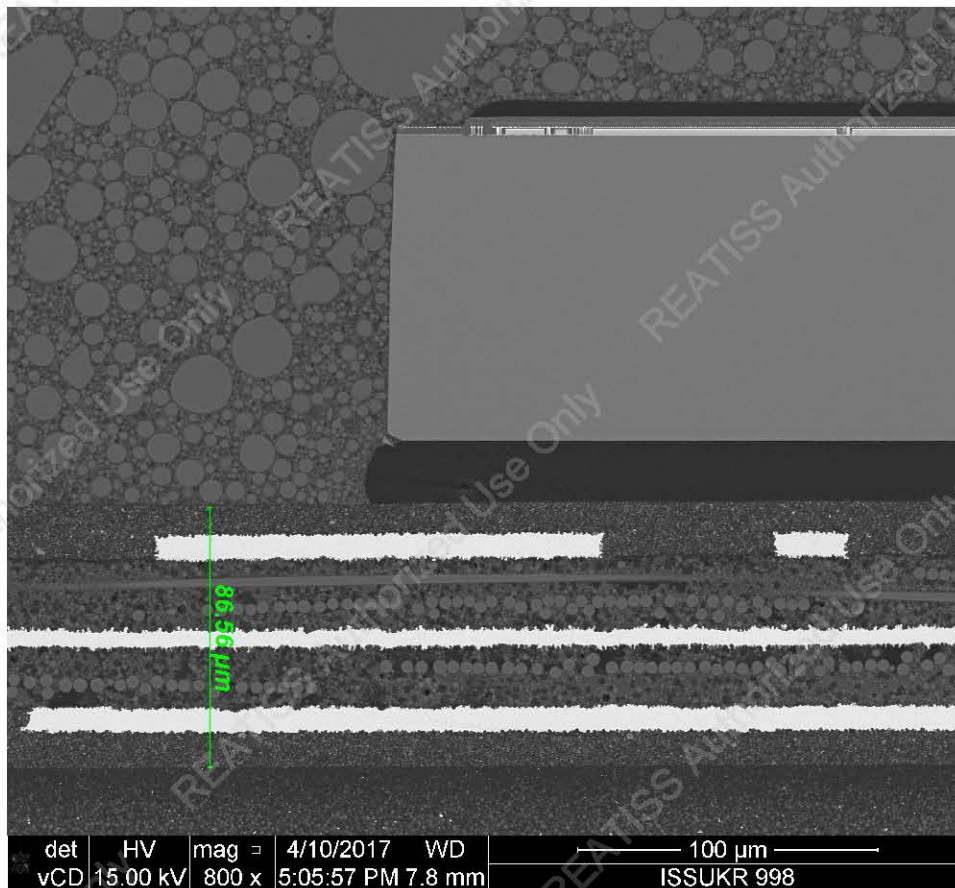


Figure 25. Memory package substrate

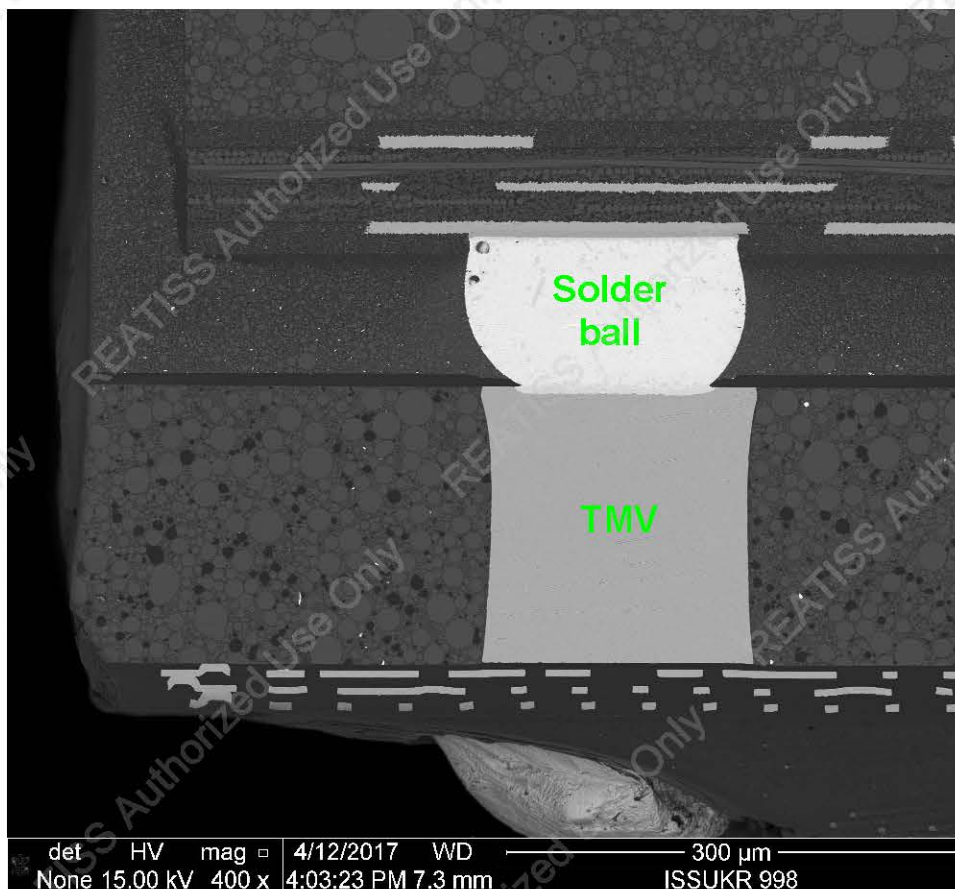


Figure 26. Package connection solder ball and through mold via (TMV)

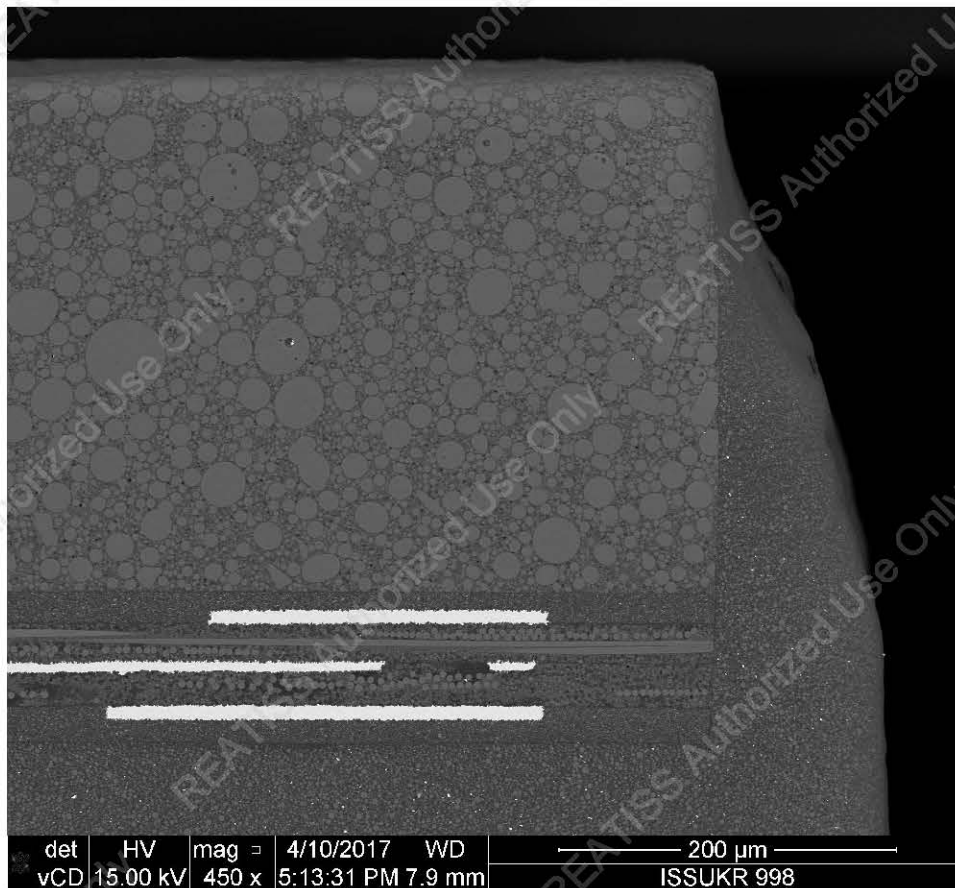


Figure 27. Memory package edge

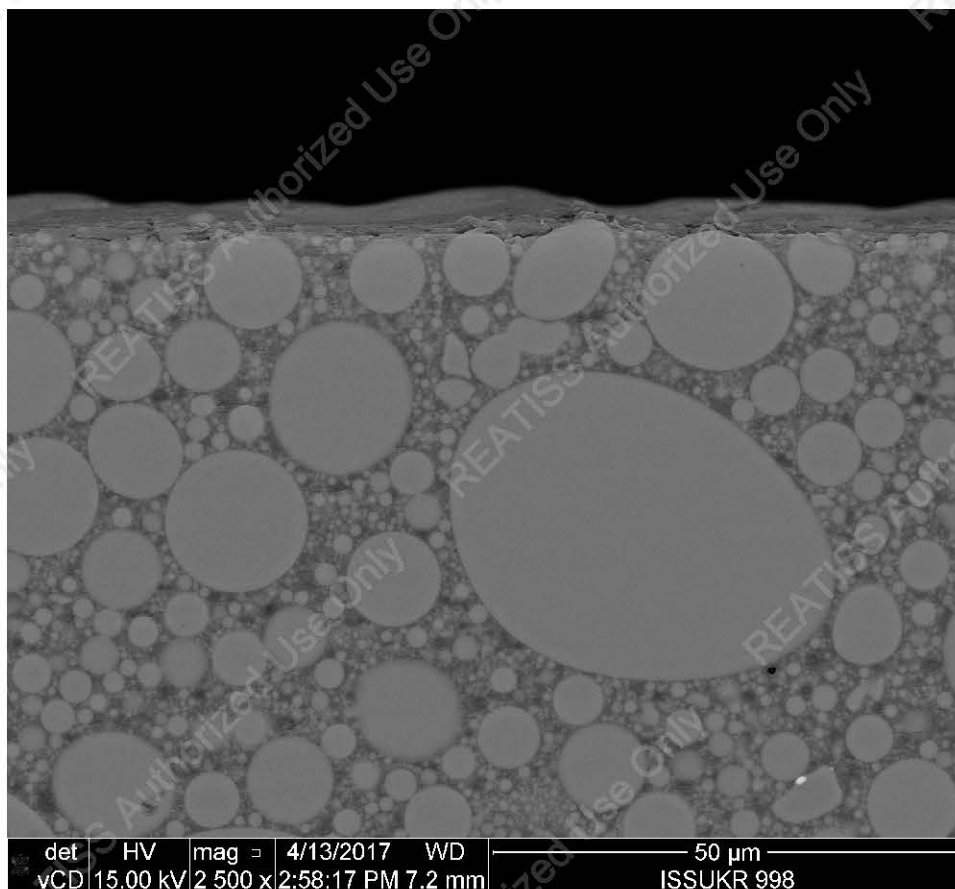


Figure 28. Memory package top surface

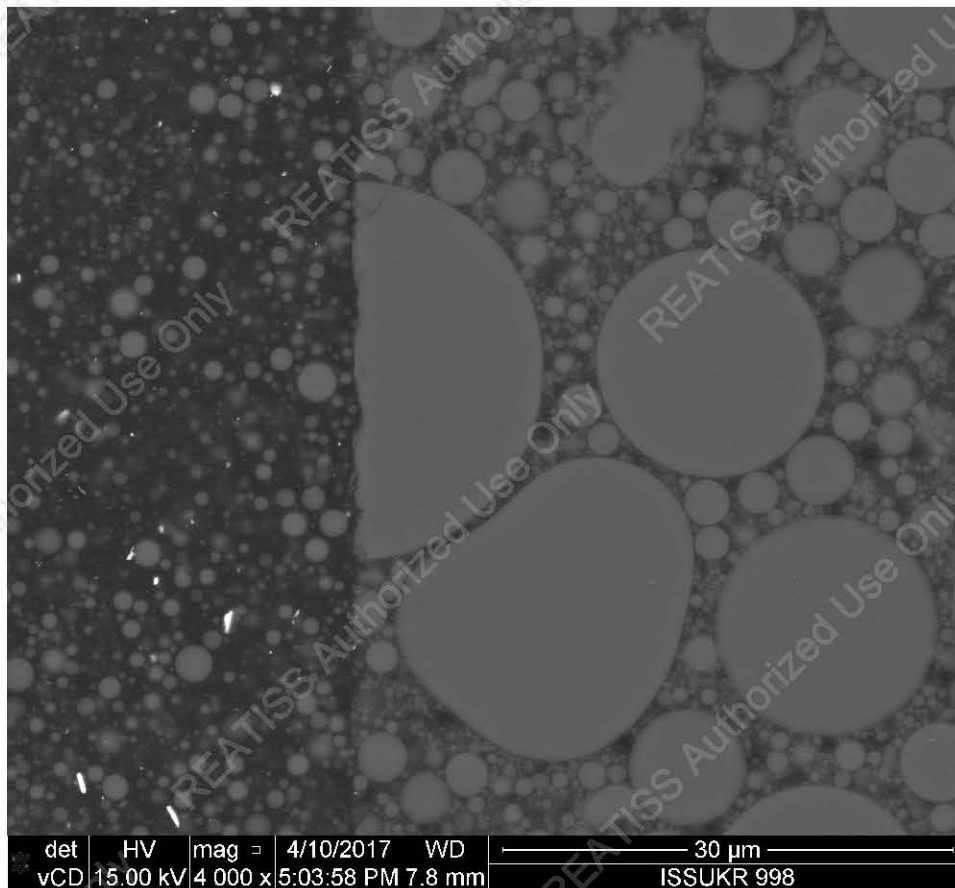


Figure 29. Memory package mold compound edge

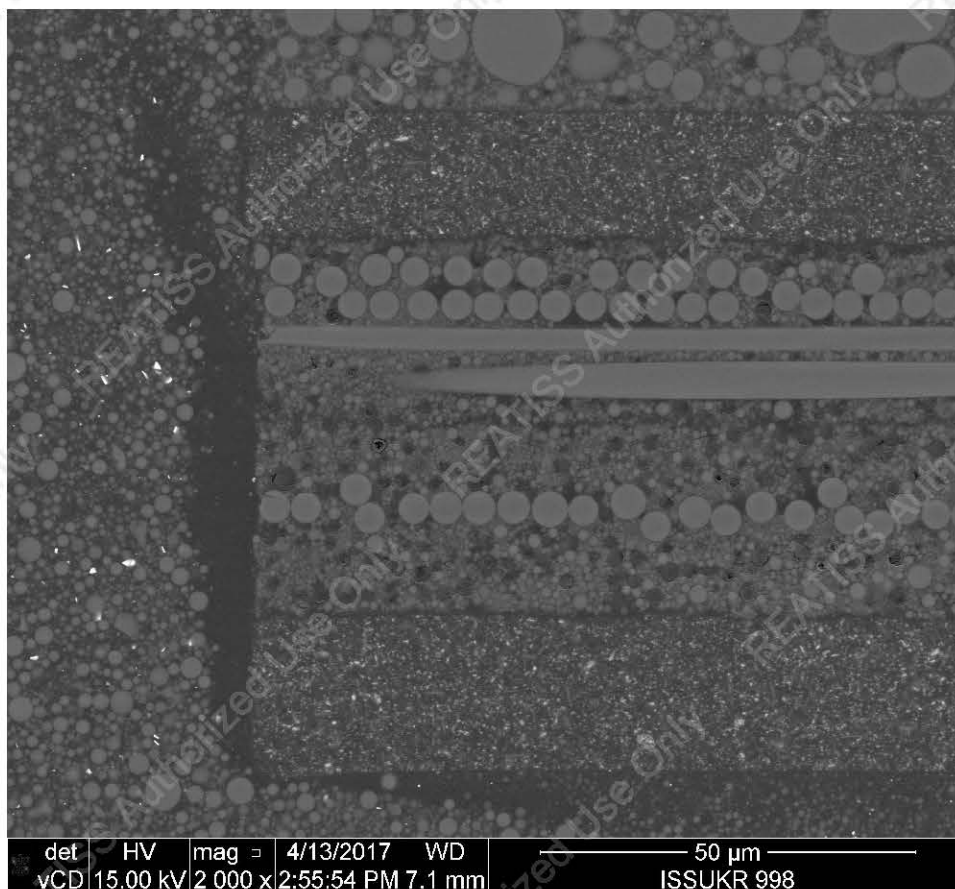


Figure 30. Memory package substrate edge

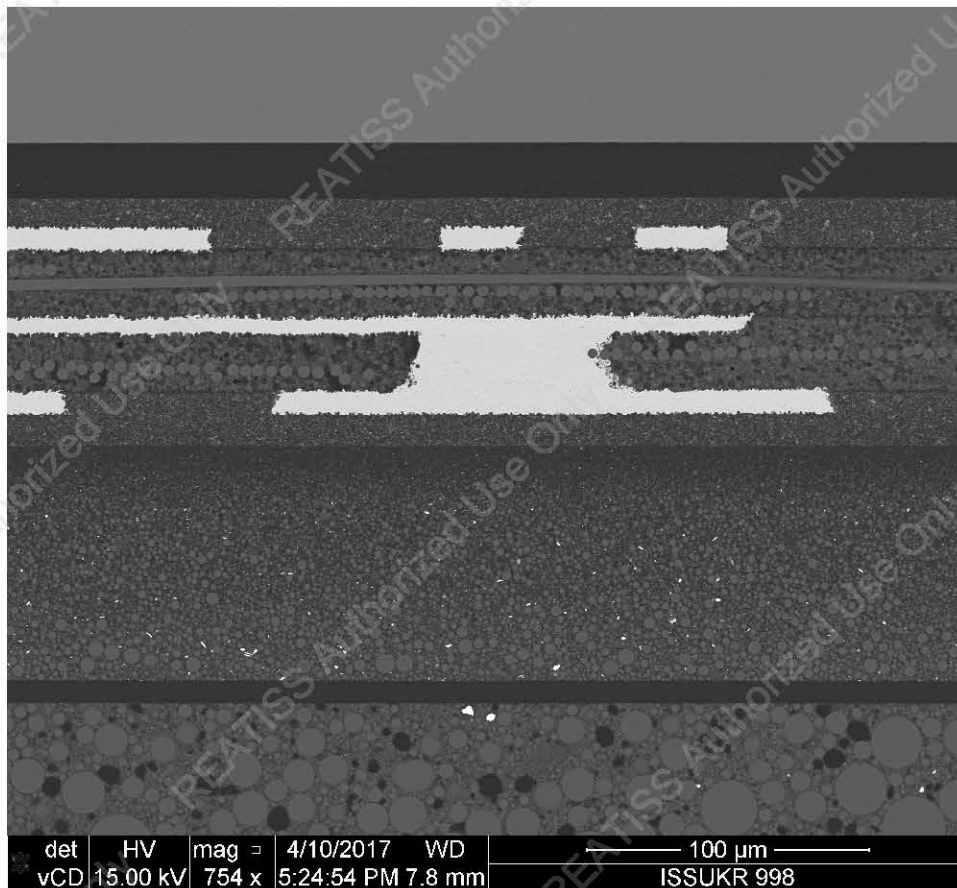


Figure 31. Memory package substrate via

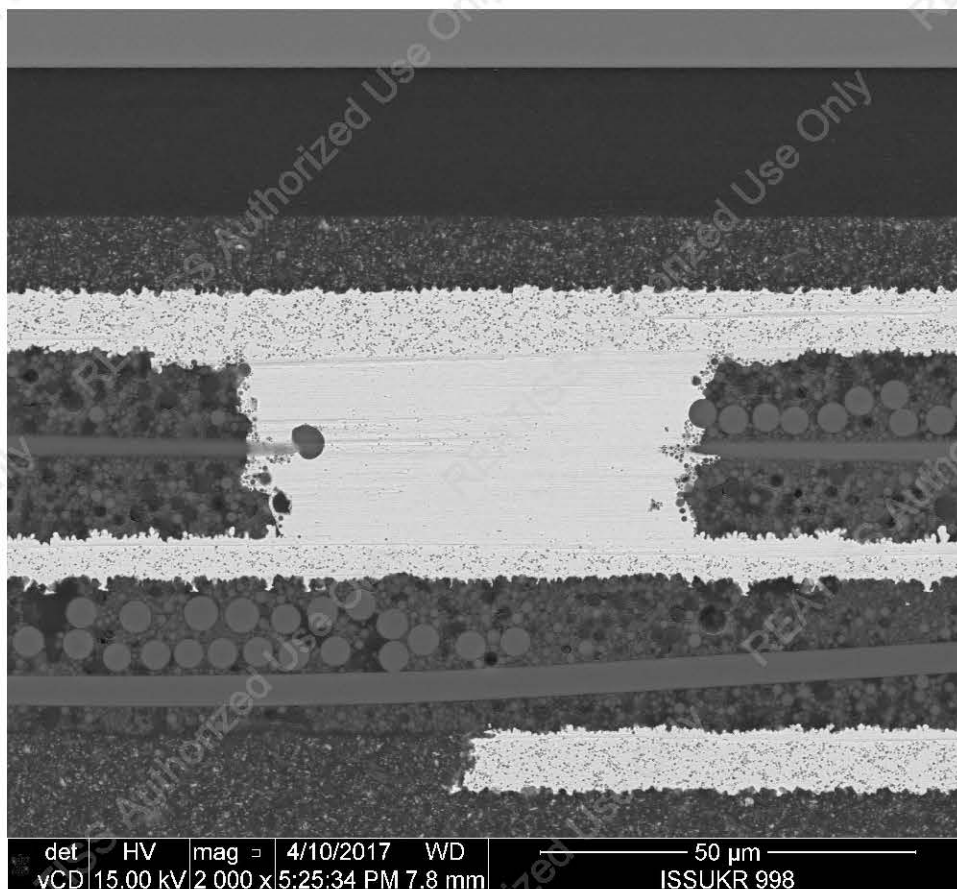


Figure 32. Memory package substrate via

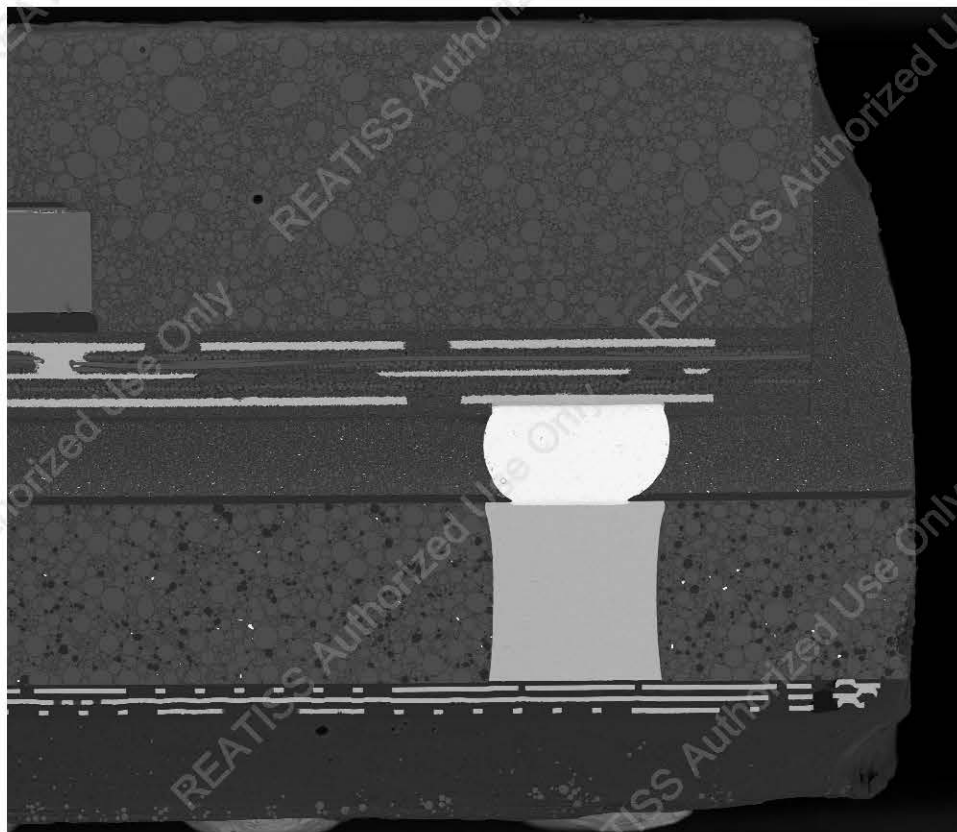


Figure 33. Package assembly edge and package connection

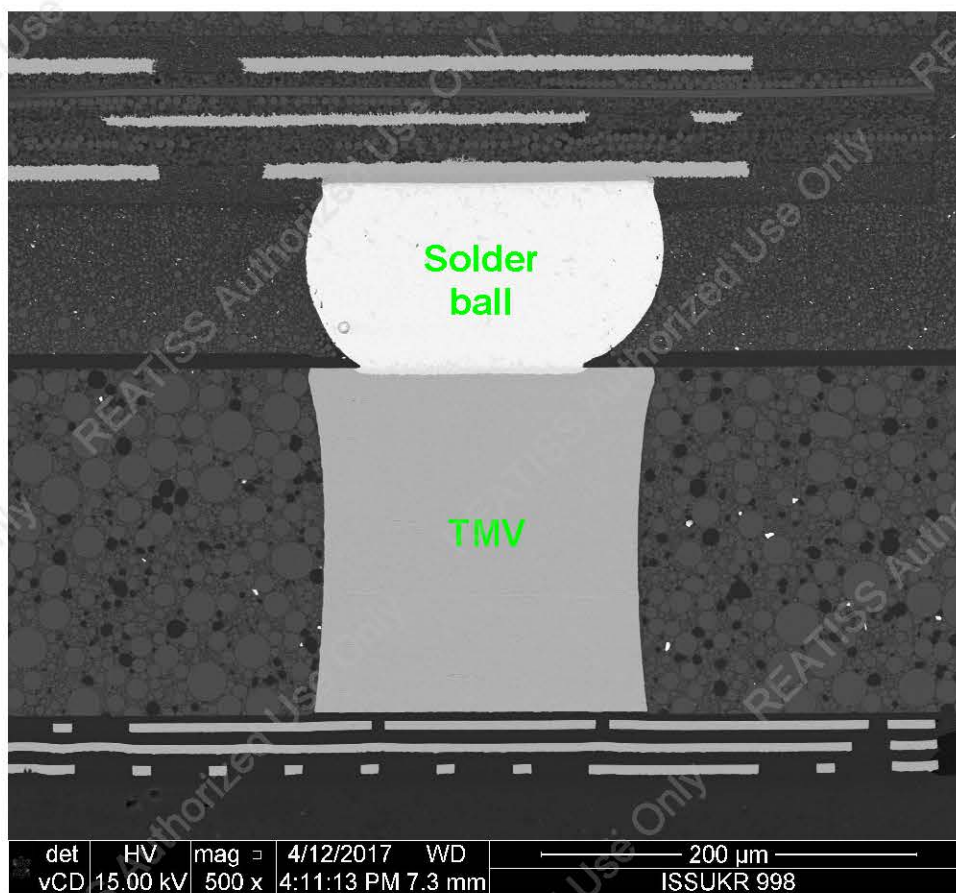


Figure 34. Package connection solder ball and through mold via (TMV)

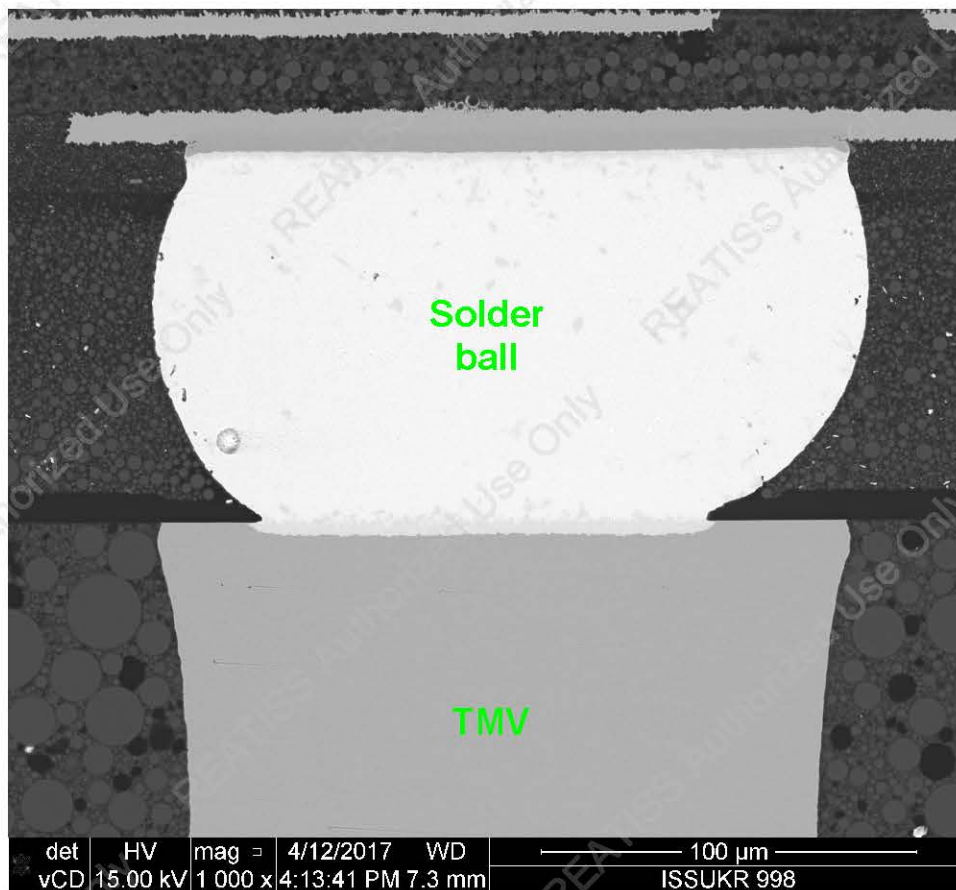


Figure 35. Memory package contact pad and package connection solder ball

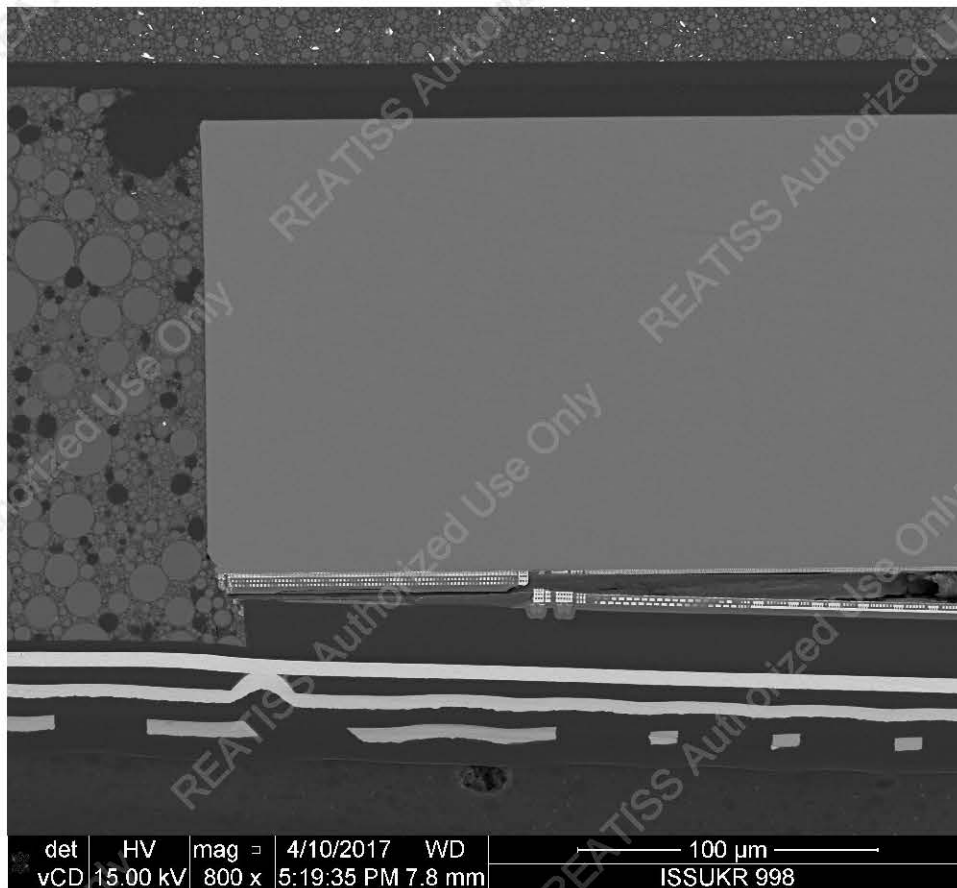


Figure 36. Processor die assembly

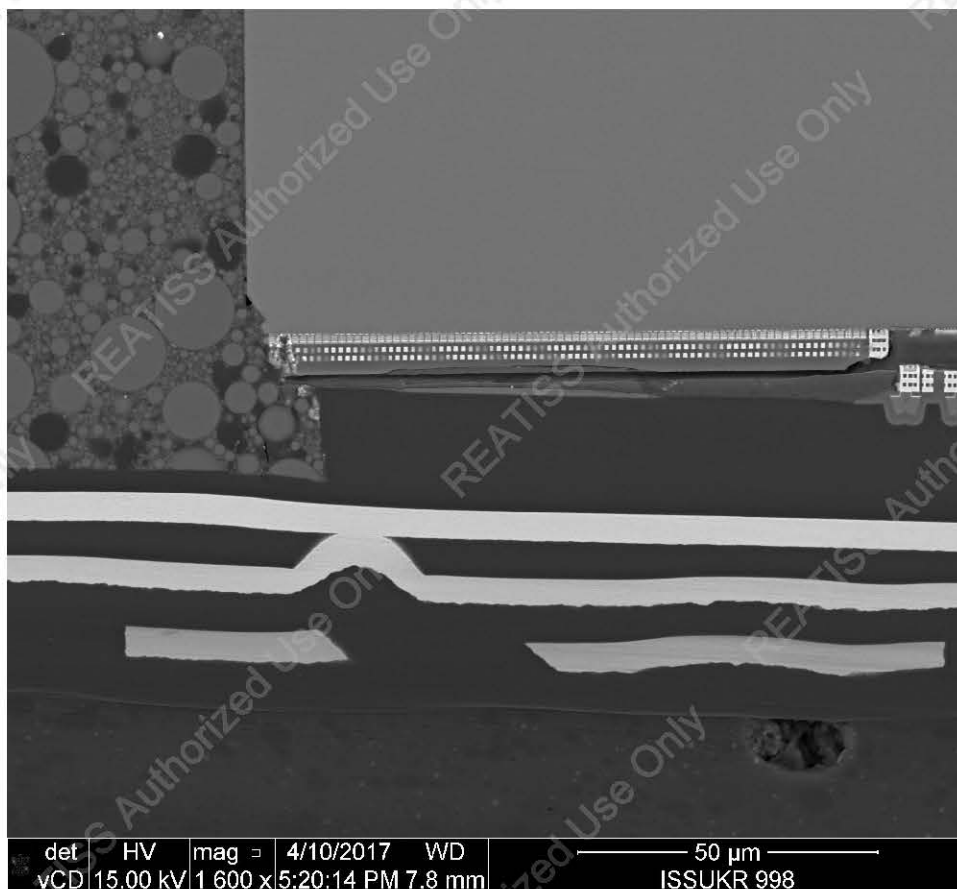


Figure 37. Processor die corner and encapsulation

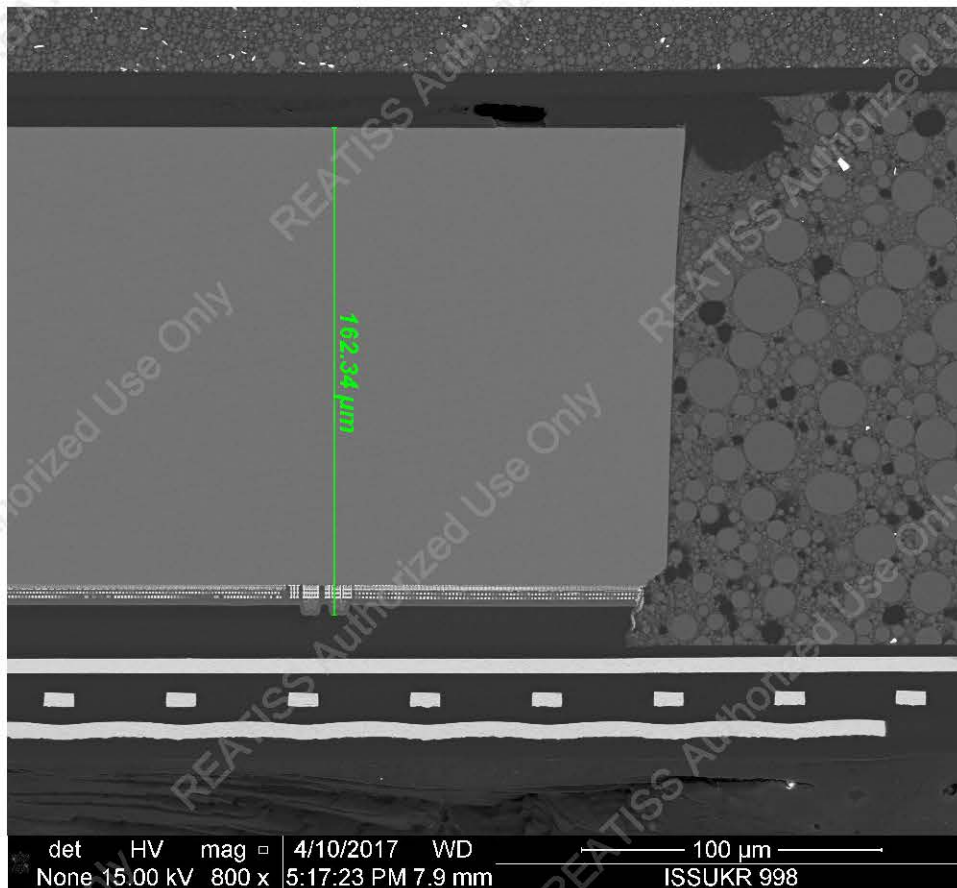


Figure 38. Processor die assembly

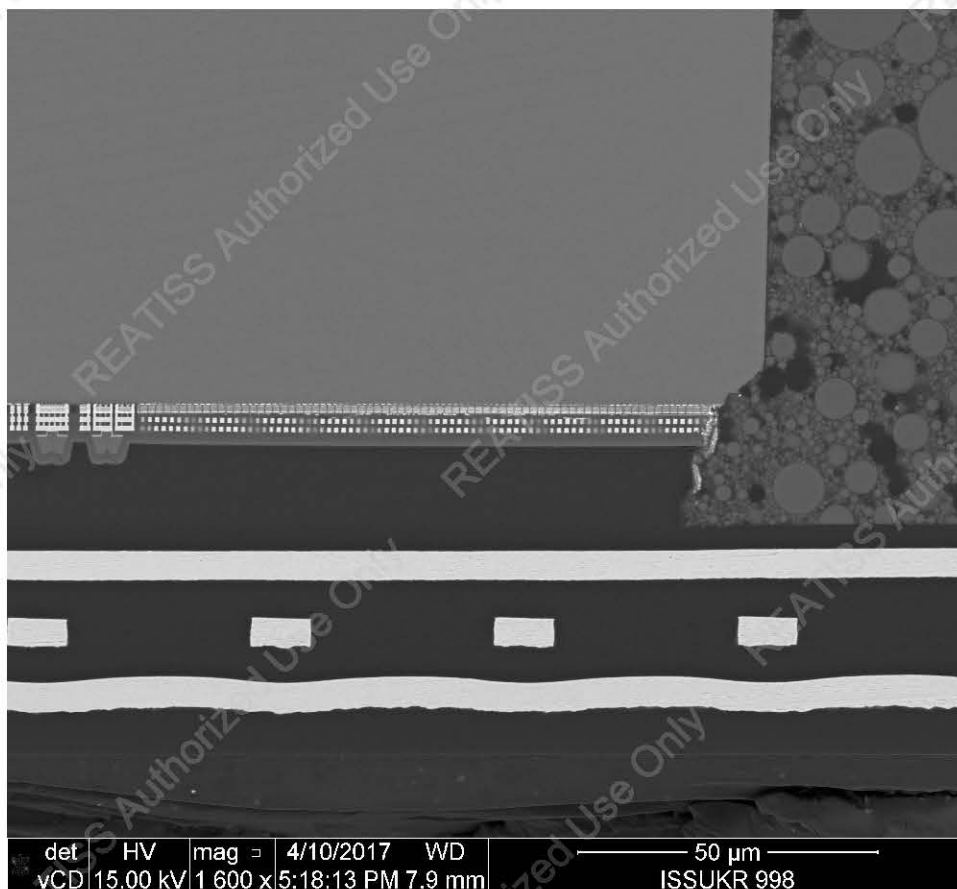


Figure 39. Processor die corner and encapsulation

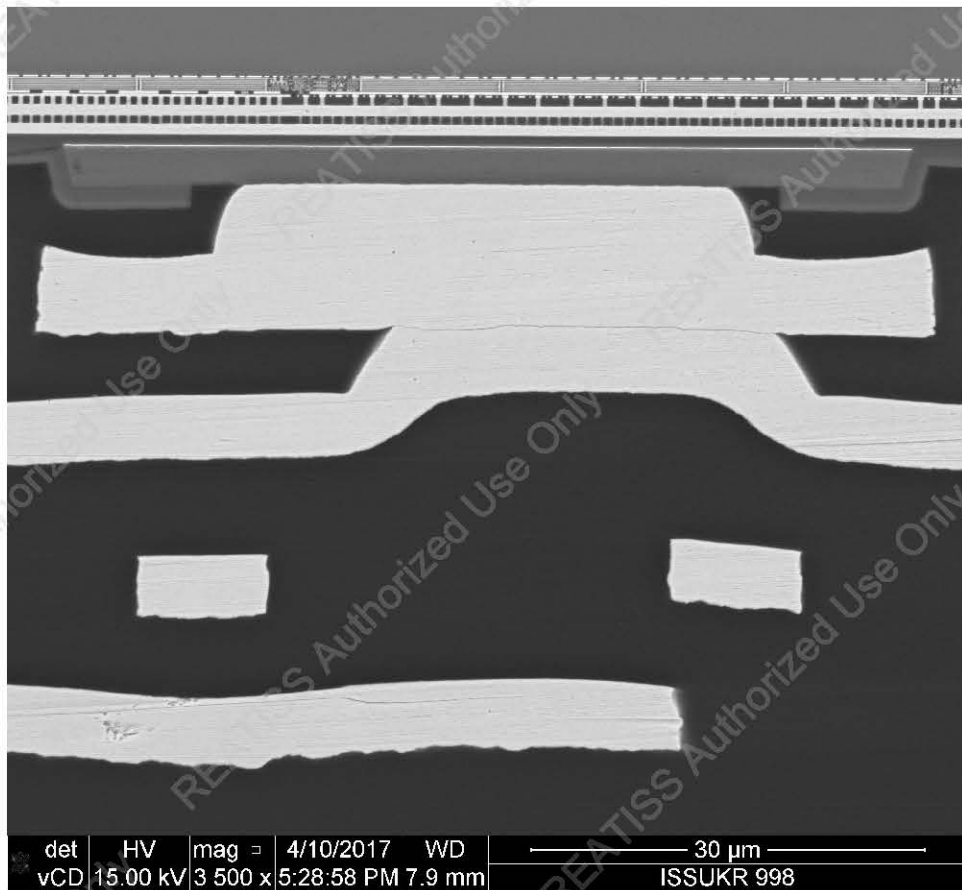


Figure 40. Processor die bond pad

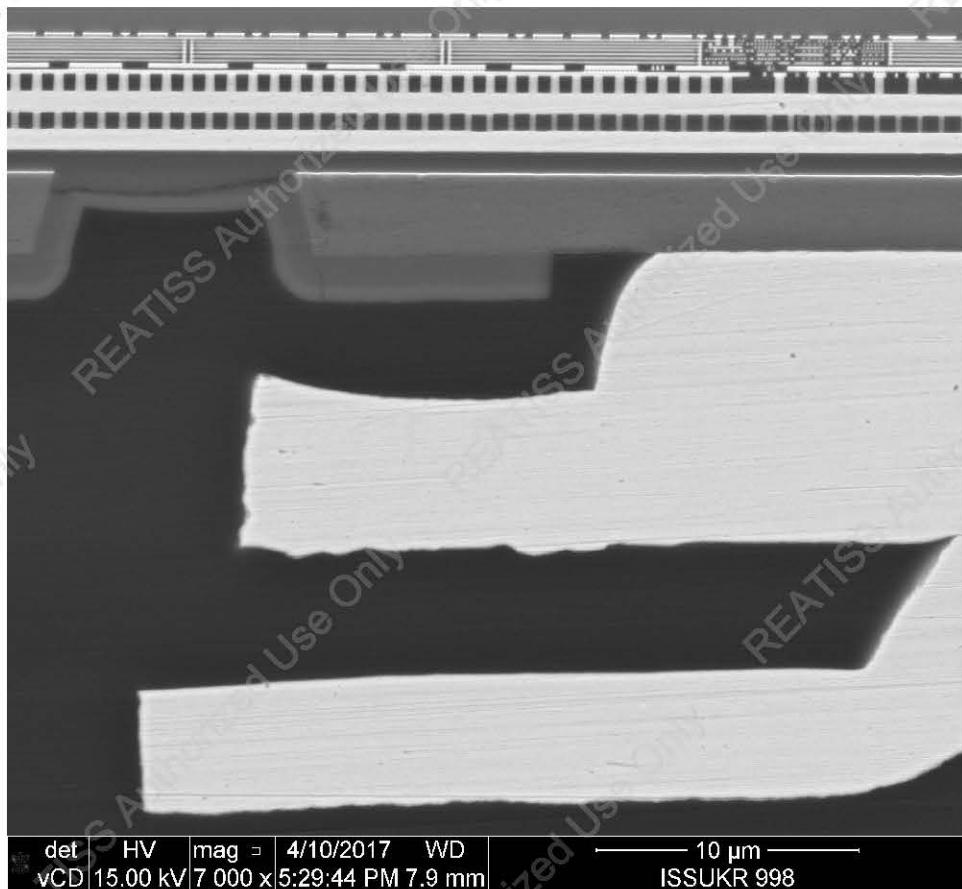


Figure 41. Processor die bond pad edge

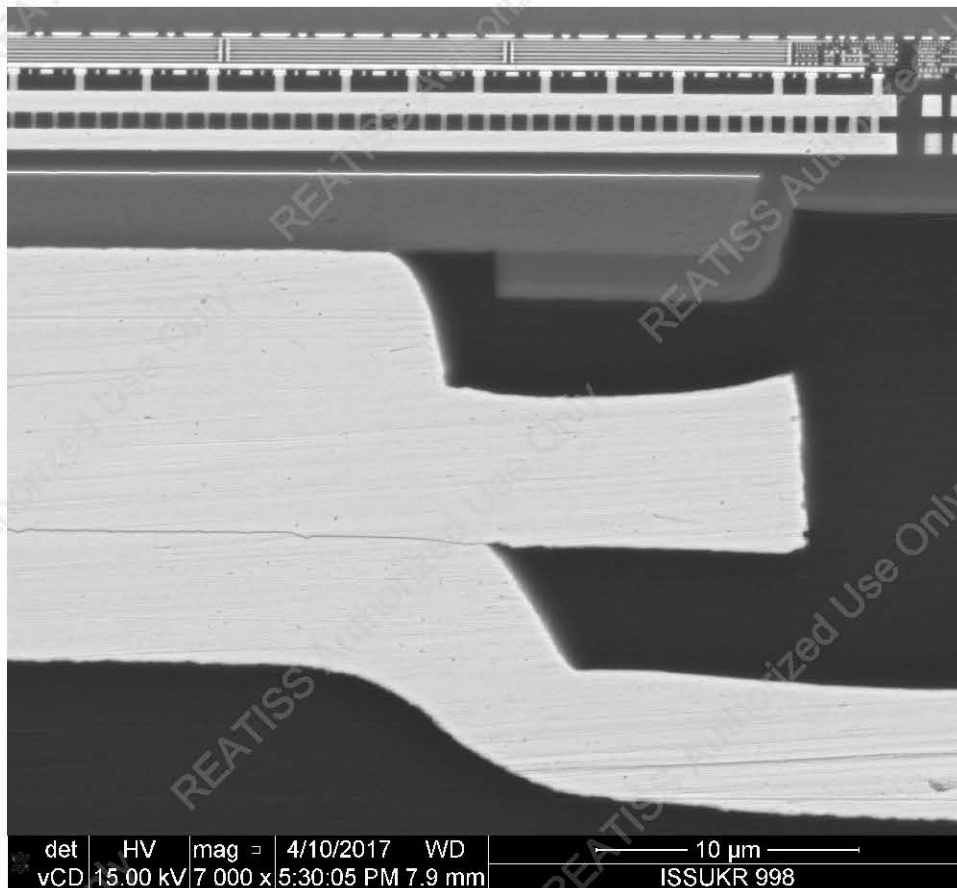


Figure 42. Processor die bond pad edge

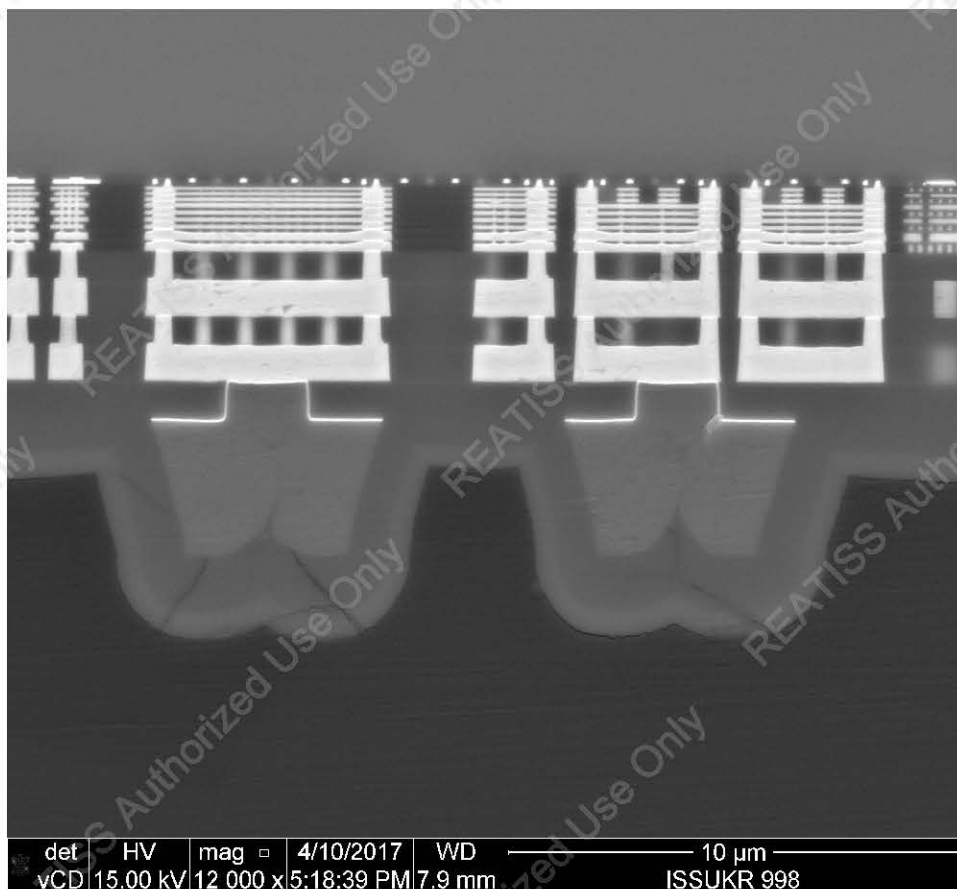


Figure 43. Processor die edge seal ring

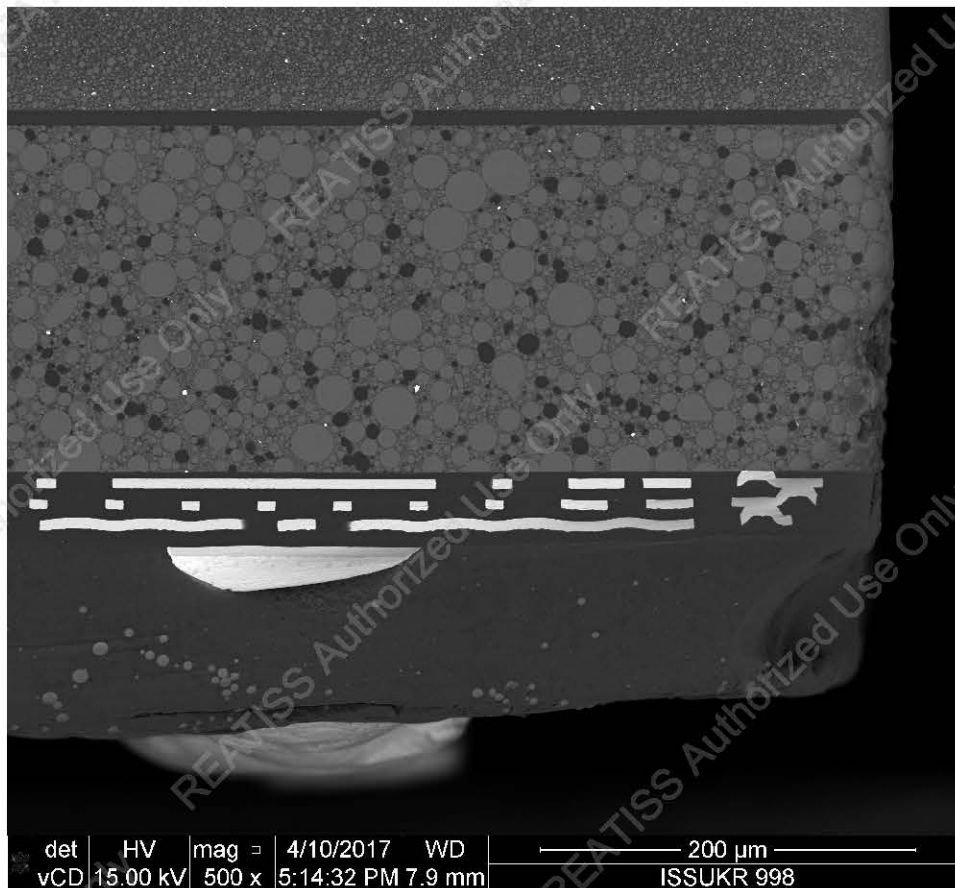


Figure 44. Processor package edge

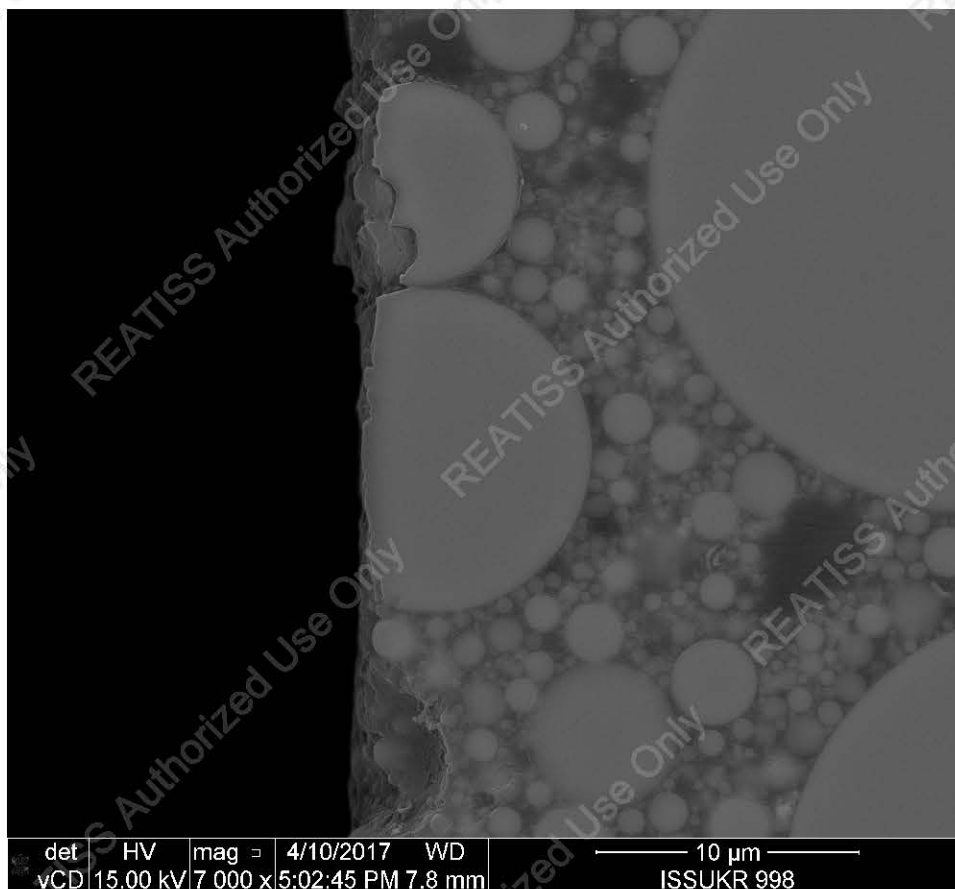


Figure 45. Processor package mold compound edge

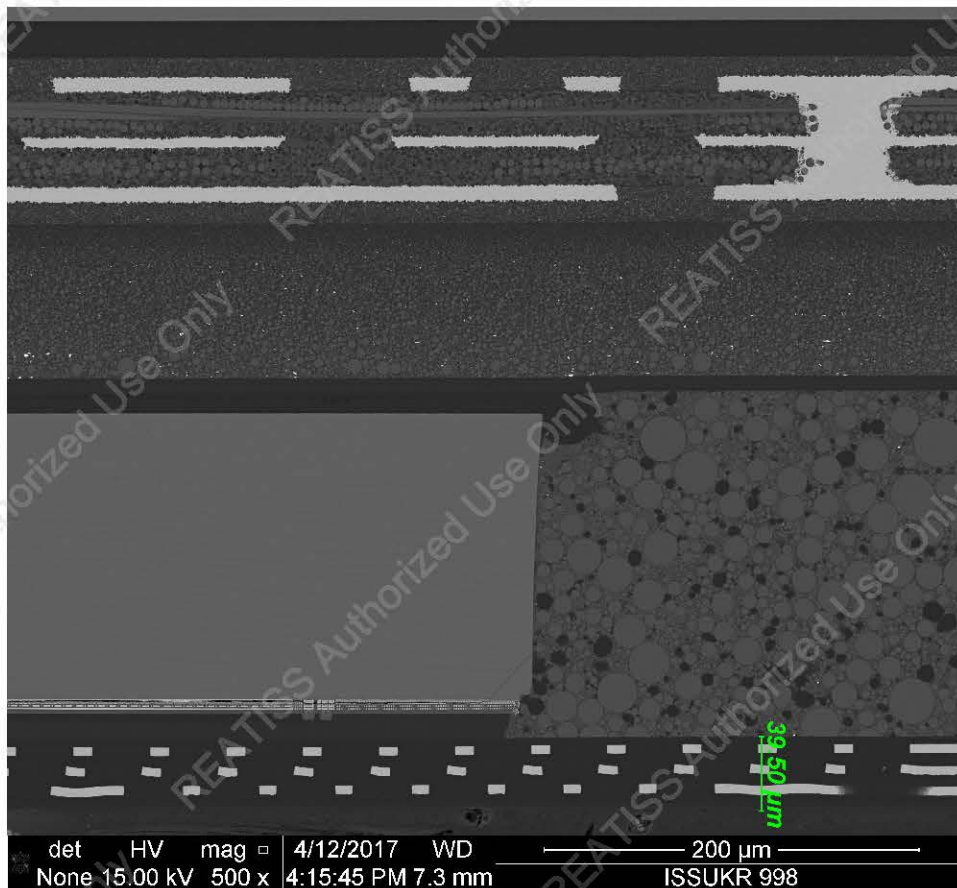


Figure 46. Processor package substrate and die

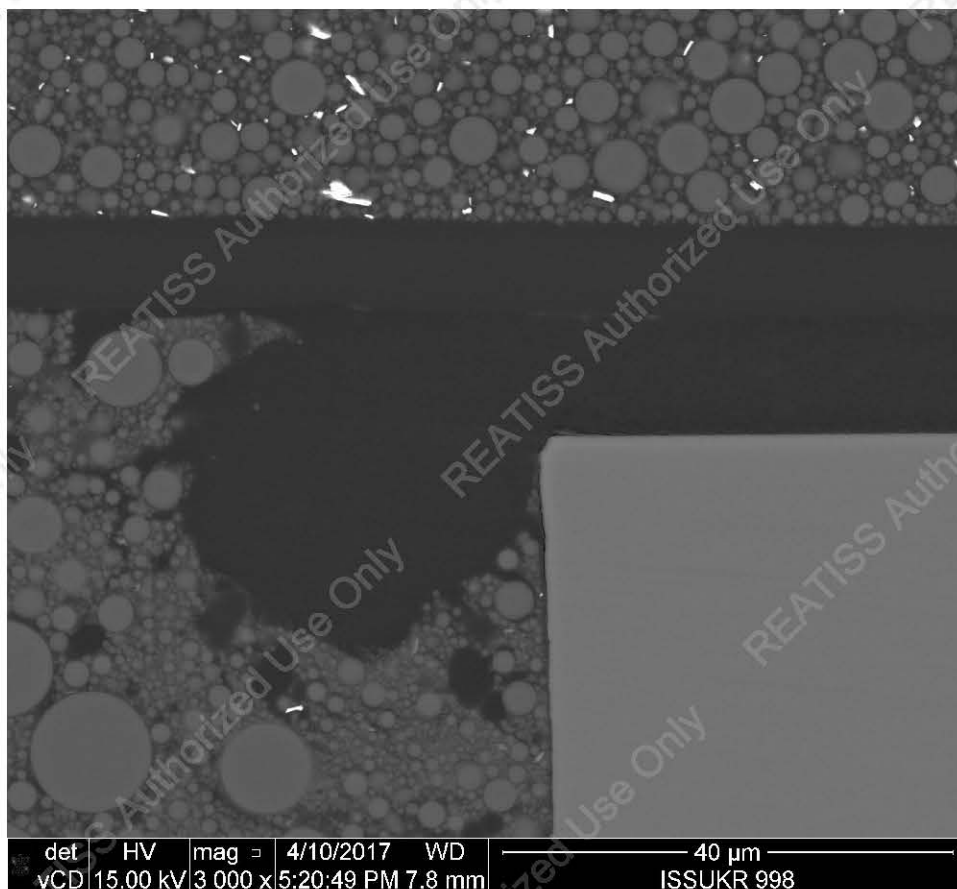


Figure 47. Processor die corner

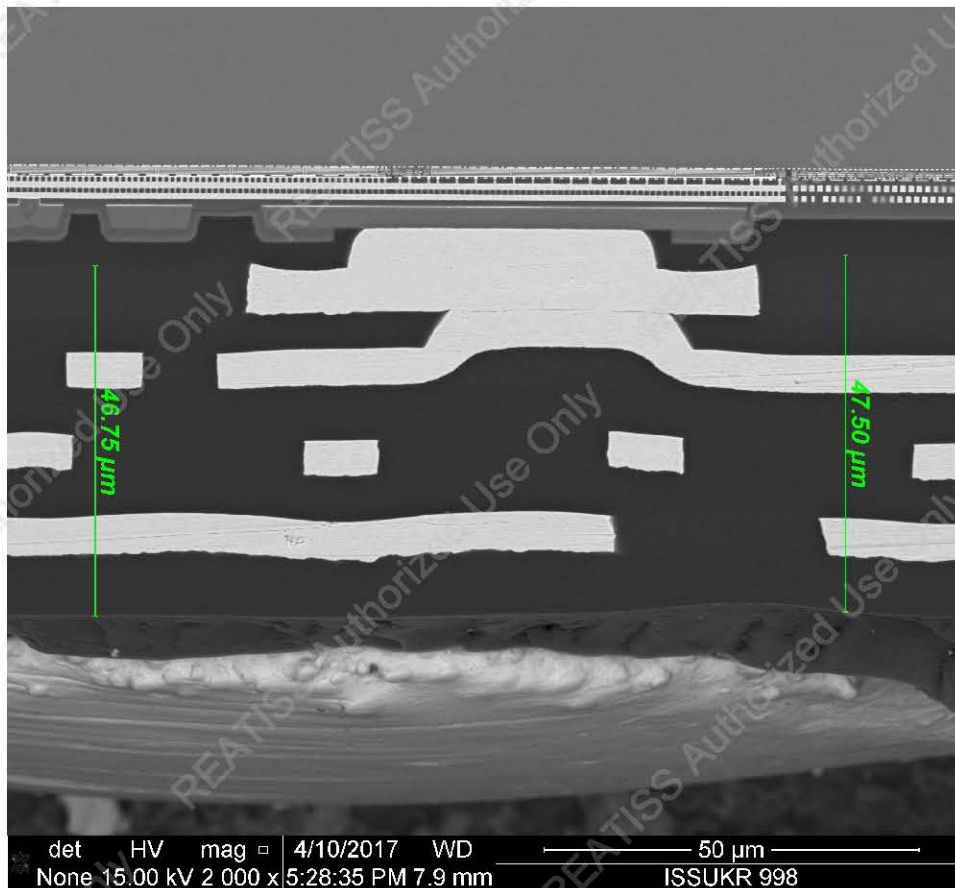


Figure 48. Processor package substrate

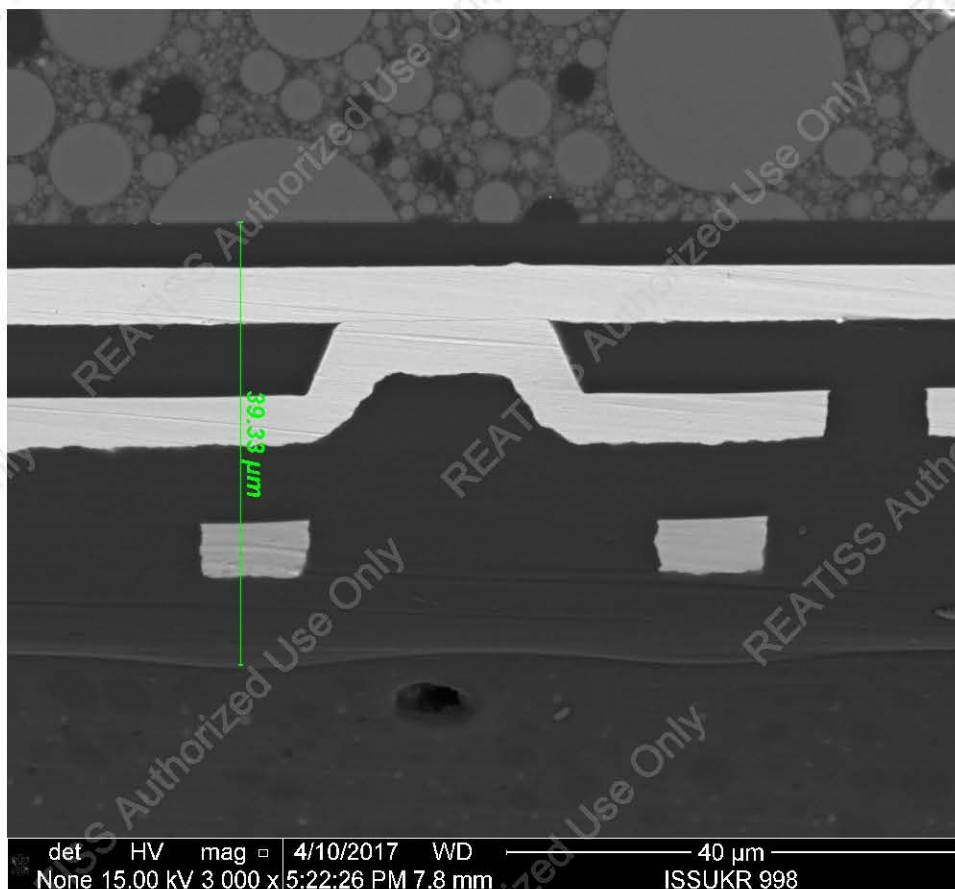


Figure 49. Processor package substrate and via

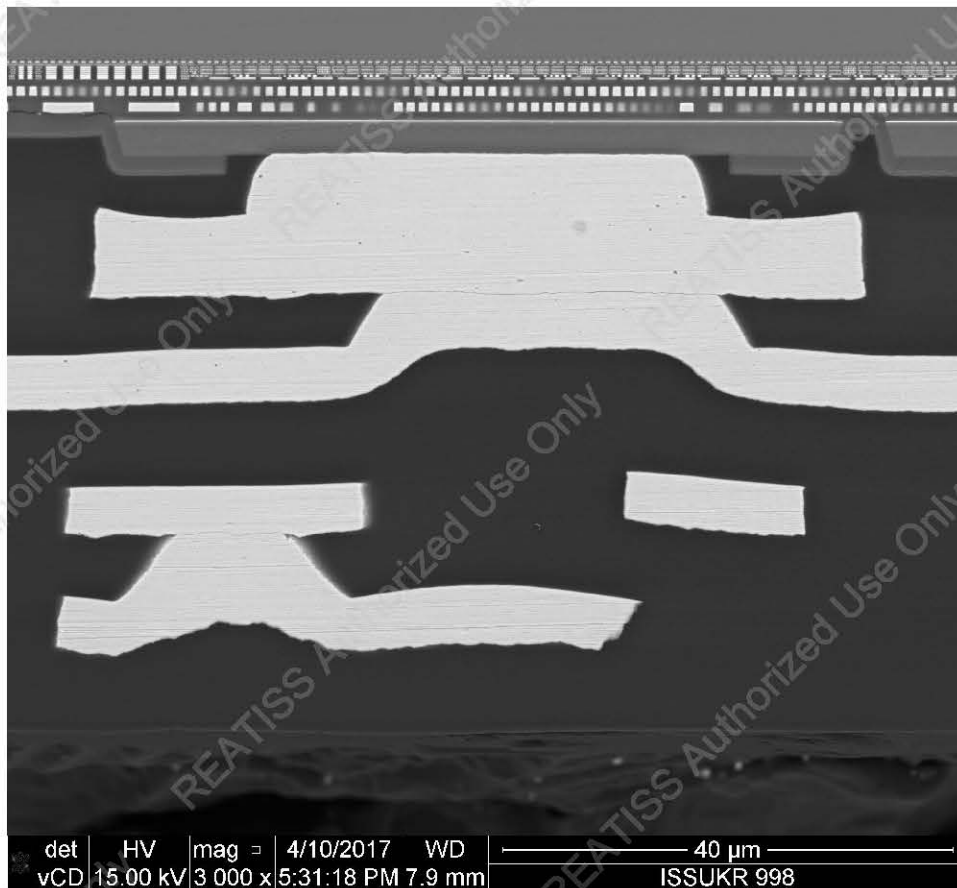


Figure 50. Processor bond pad and package substrate via

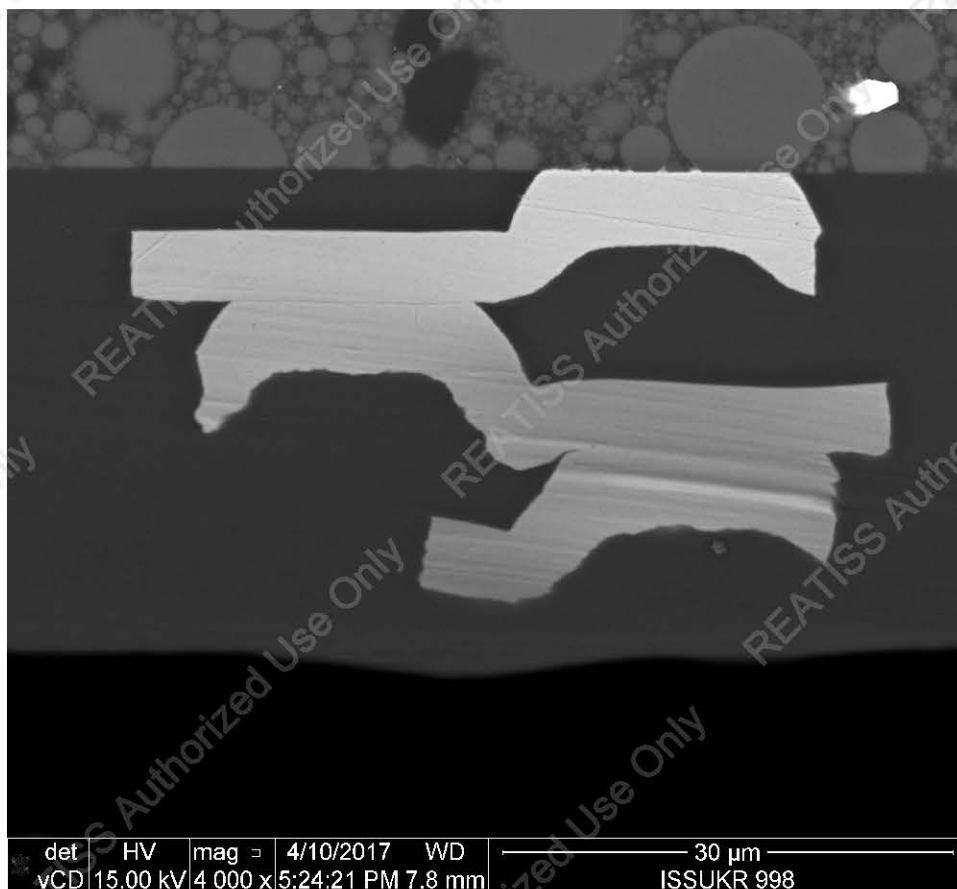


Figure 51. Processor package vias

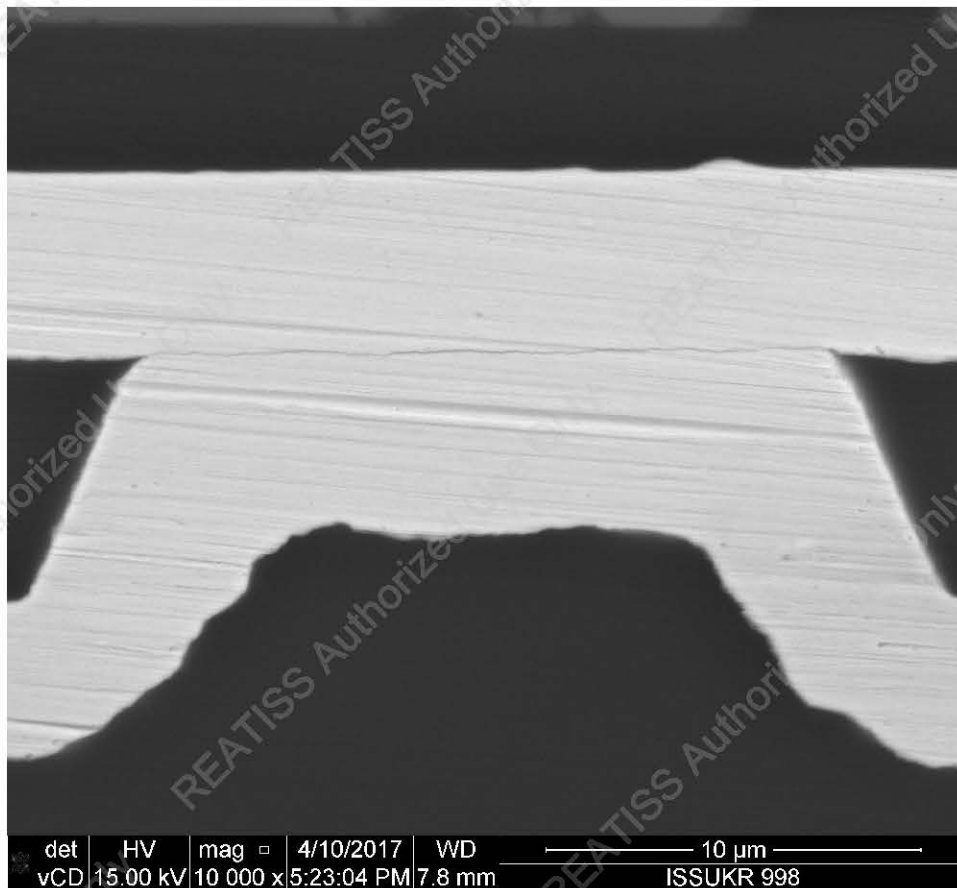


Figure 52. Processor package substrate via

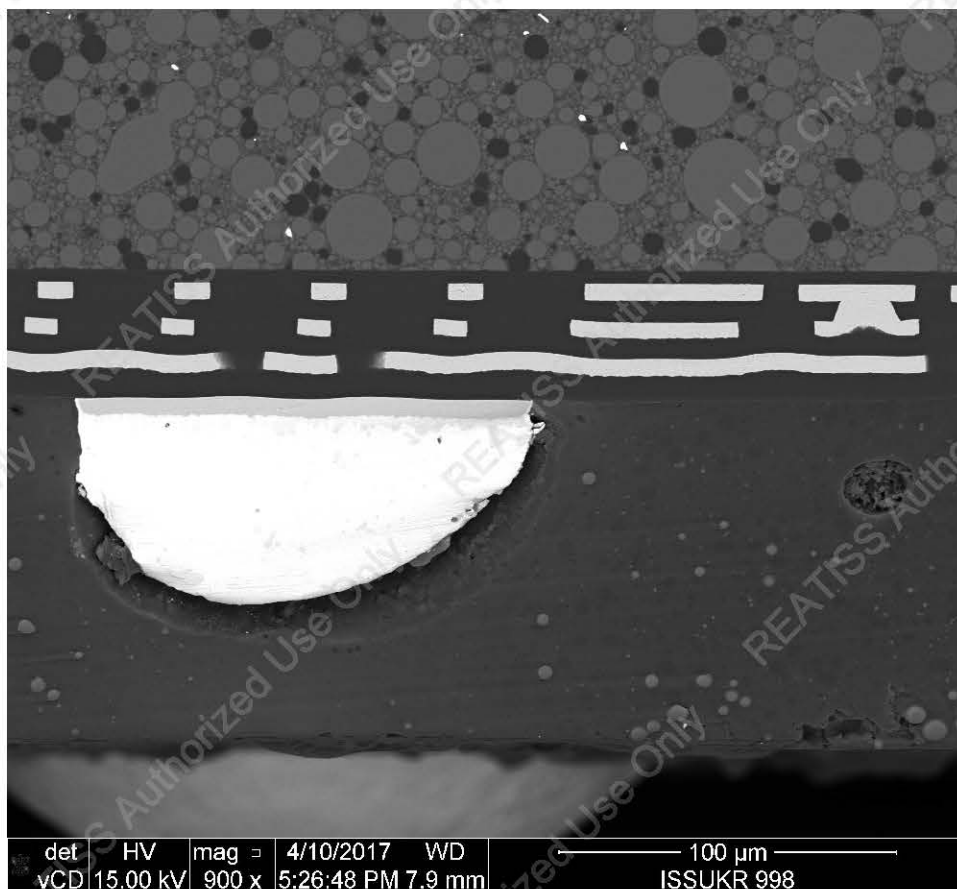


Figure 53. Processor contact pad and ball

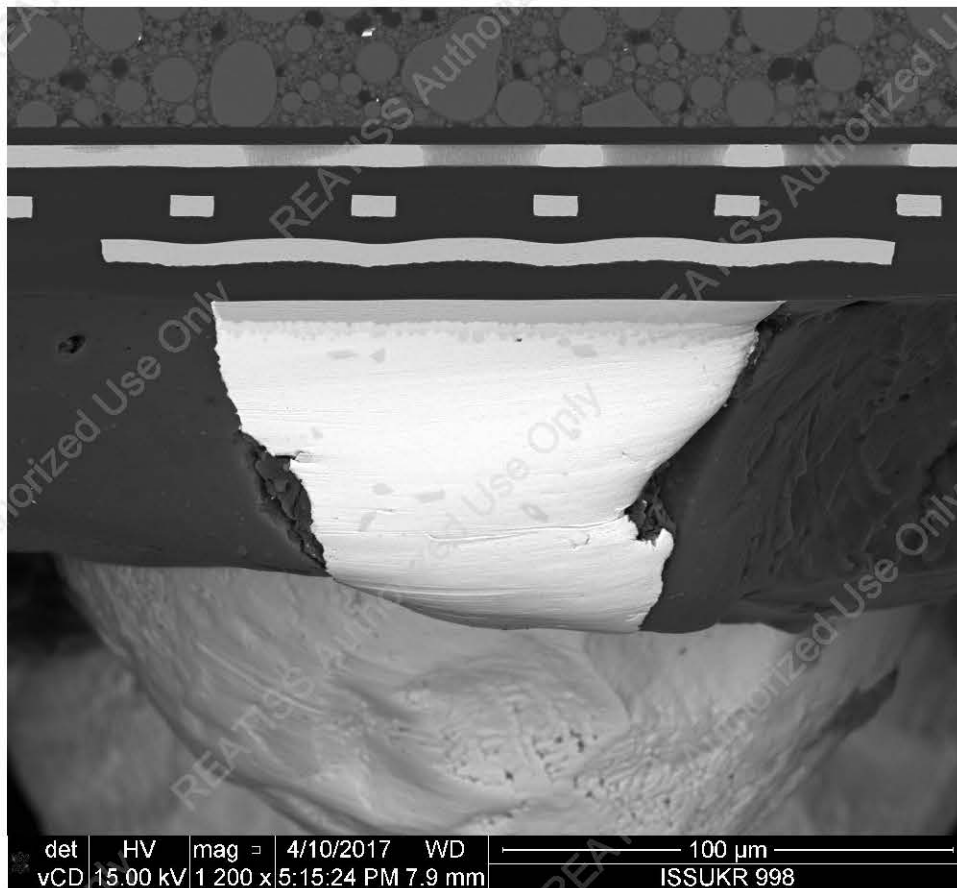


Figure 54. Processor contact pad and ball

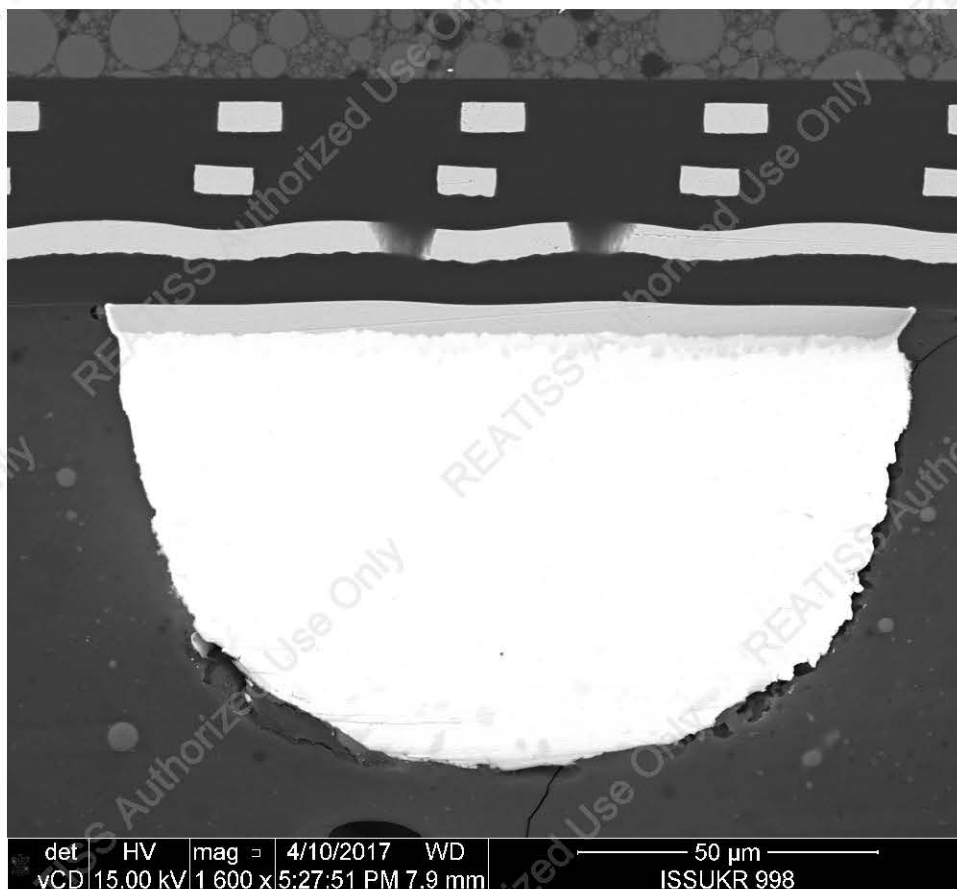


Figure 55. Processor contact pad and ball

Package Material Analysis



Figure 56. Processor die bond pad and via



Figure 57. Layered EDX map of processor die bond pad and via

Al K series

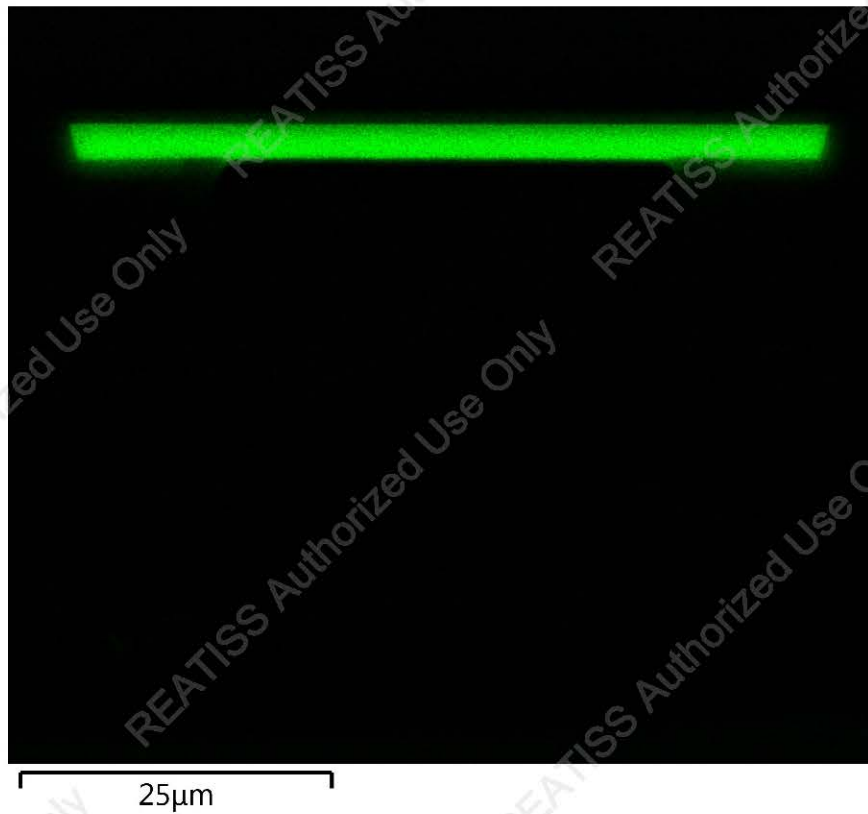


Figure 58. Aluminum EDX map layer

Ti K series

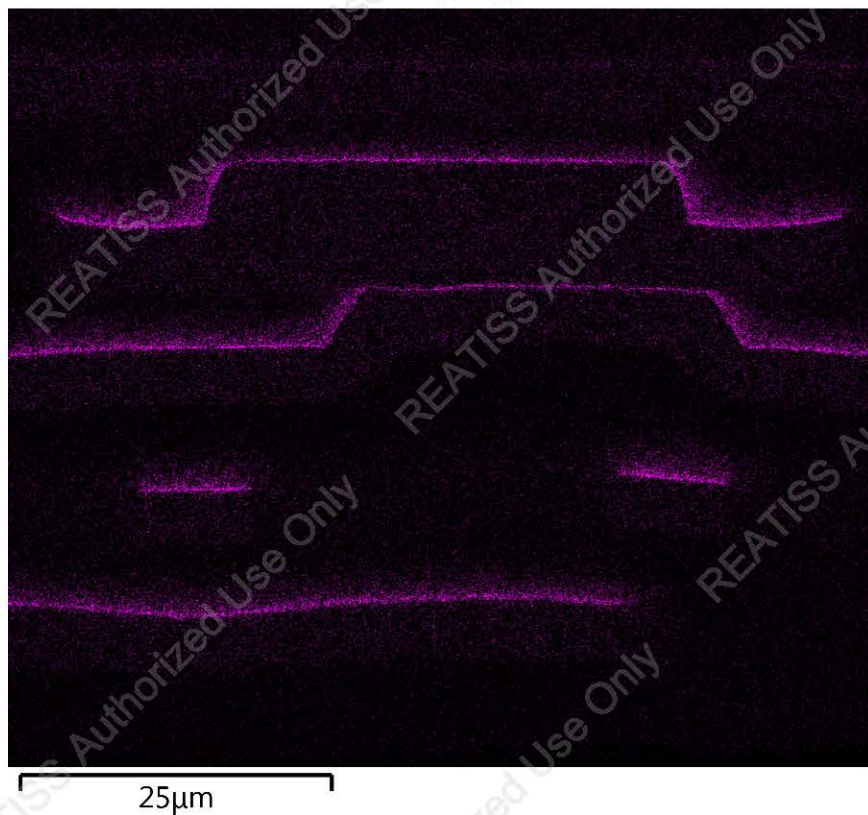


Figure 59. Titanium EDX map layer

Cu K series

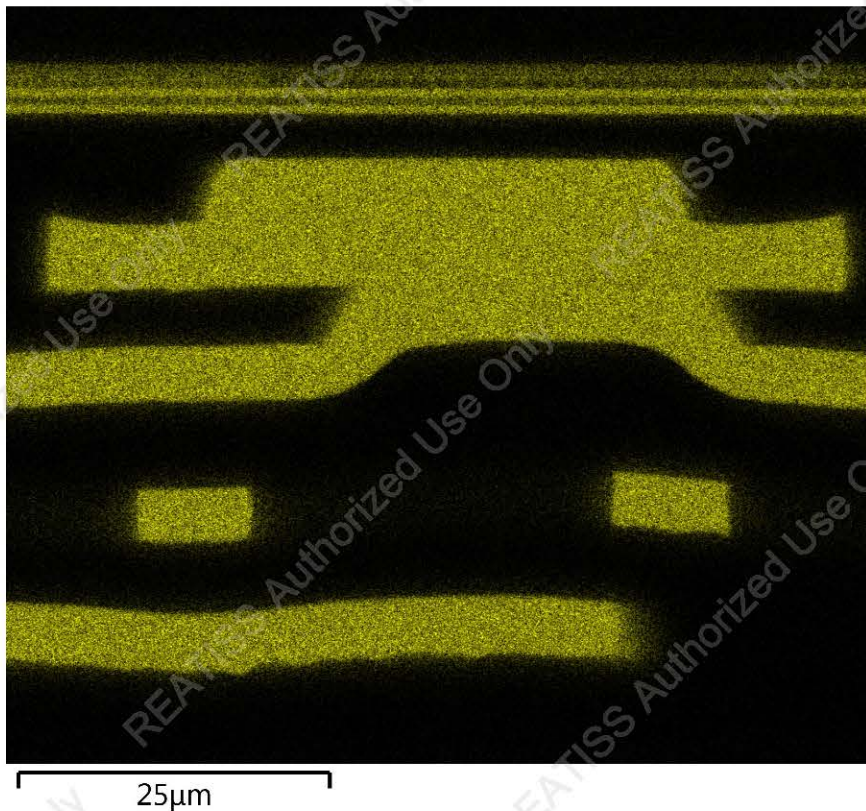


Figure 60. Copper EDX map layer

Si K series

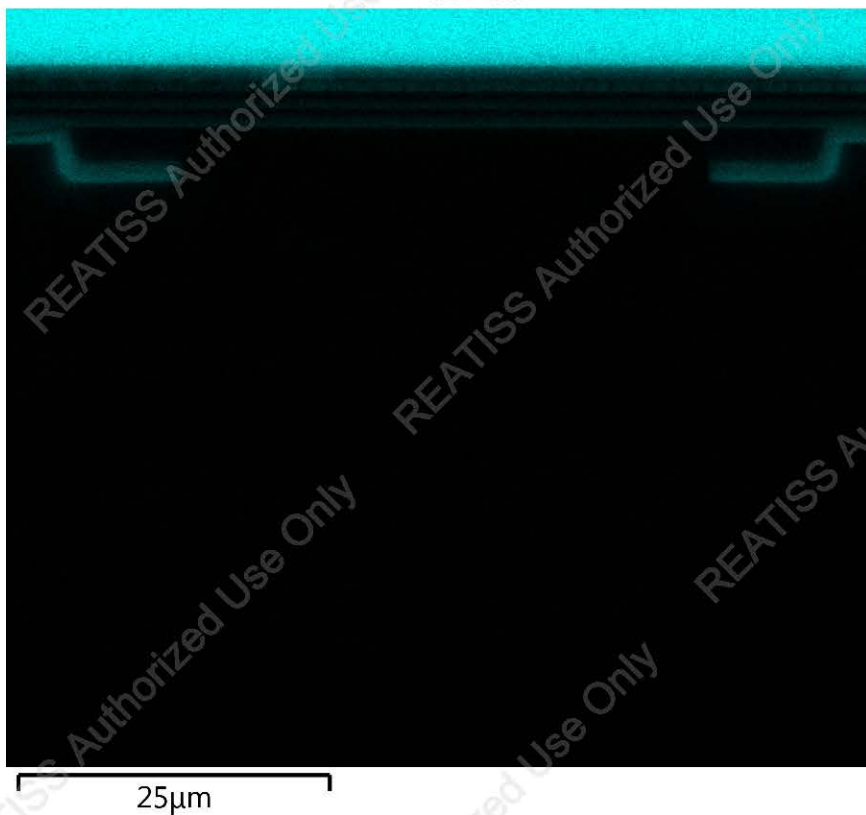


Figure 61. Silicon EDX map layer

O K series

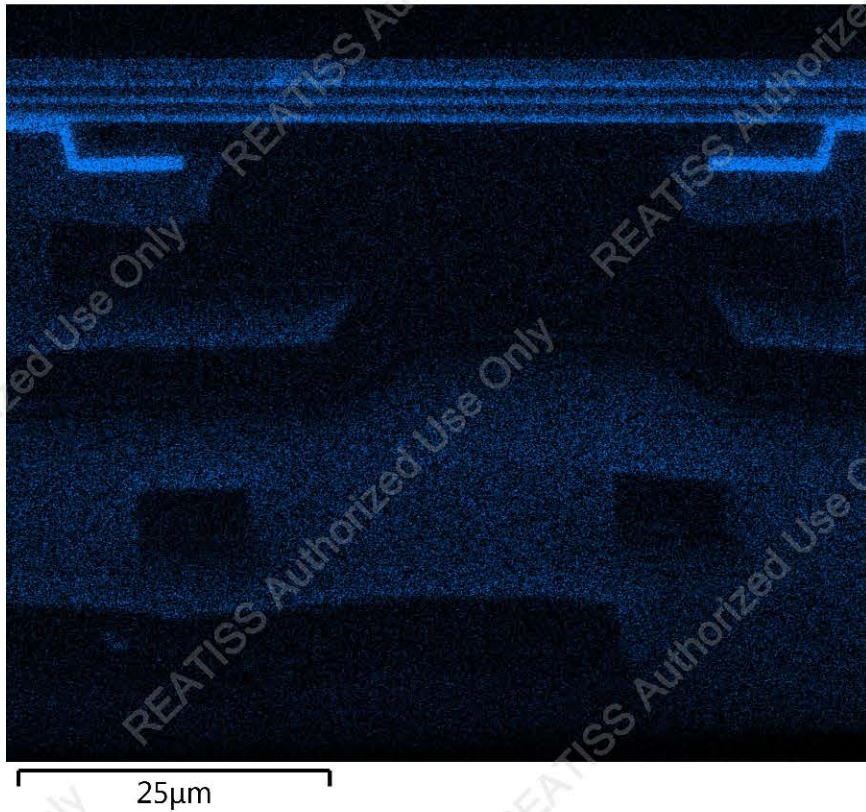


Figure 62. Oxygen EDX map layer

C K series

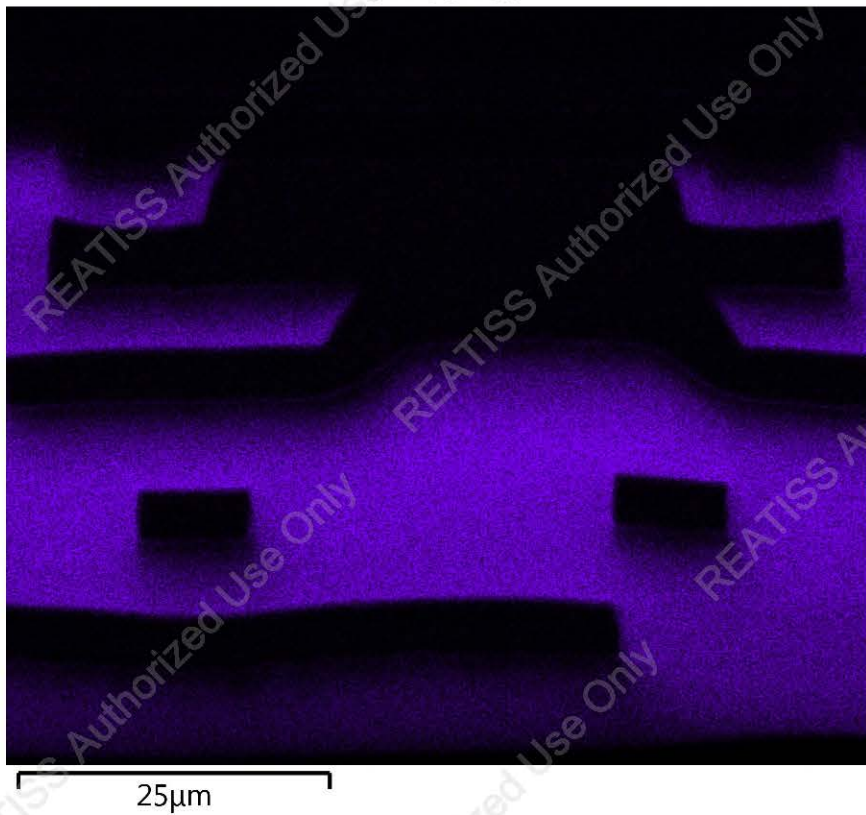


Figure 63. Carbon EDX map layer

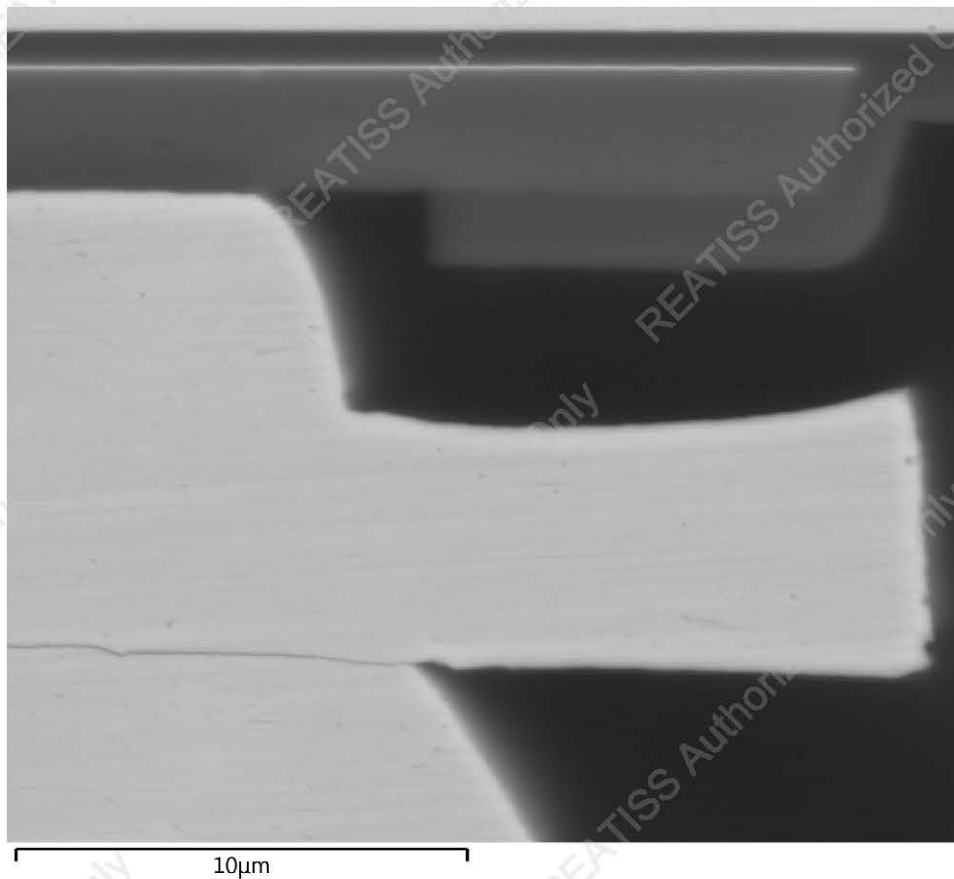


Figure 64. Processor die bond pad edge



Figure 65. Layered EDX map of processor die bond pad edge

Al K series

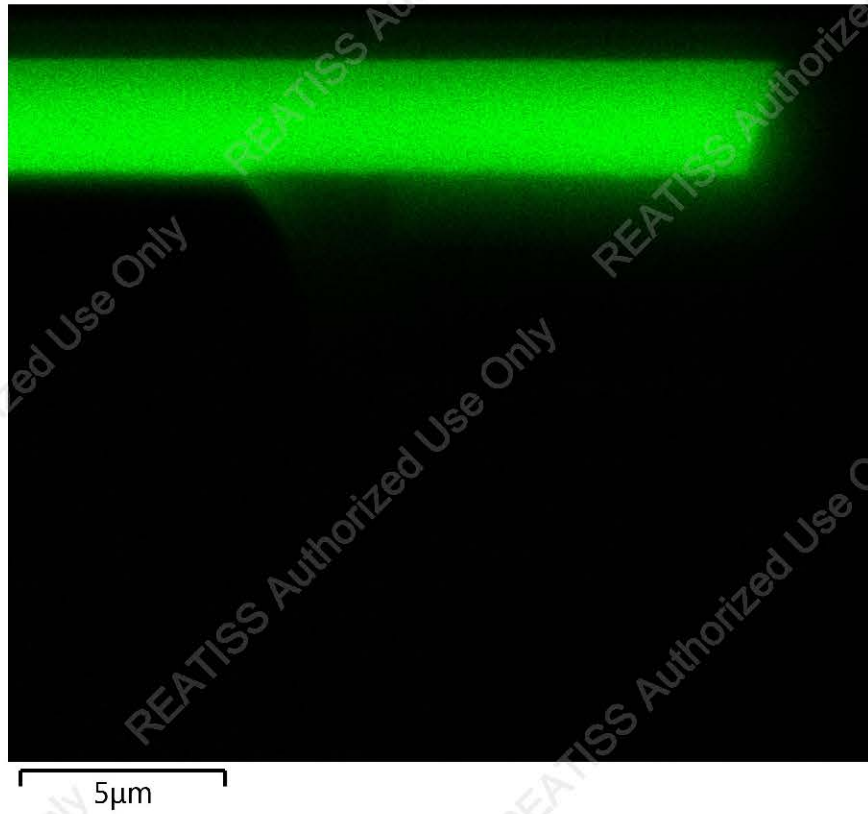


Figure 66. Aluminum EDX map layer

Cu K series

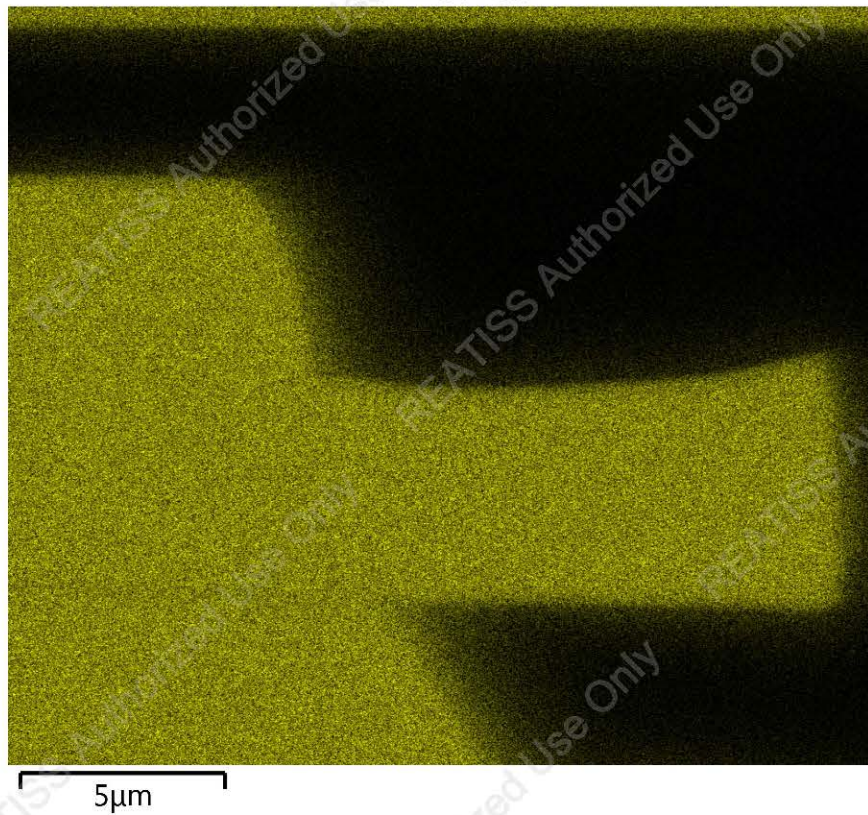


Figure 67. Copper EDX map layer

Ti K series

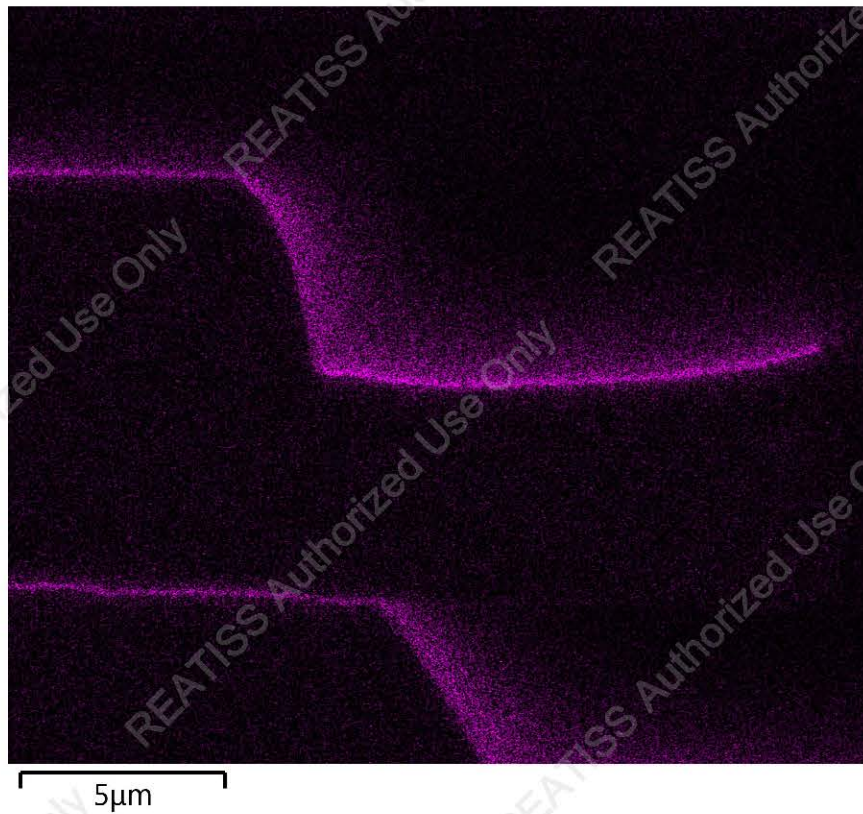


Figure 68. Titanium EDX map layer

N K series

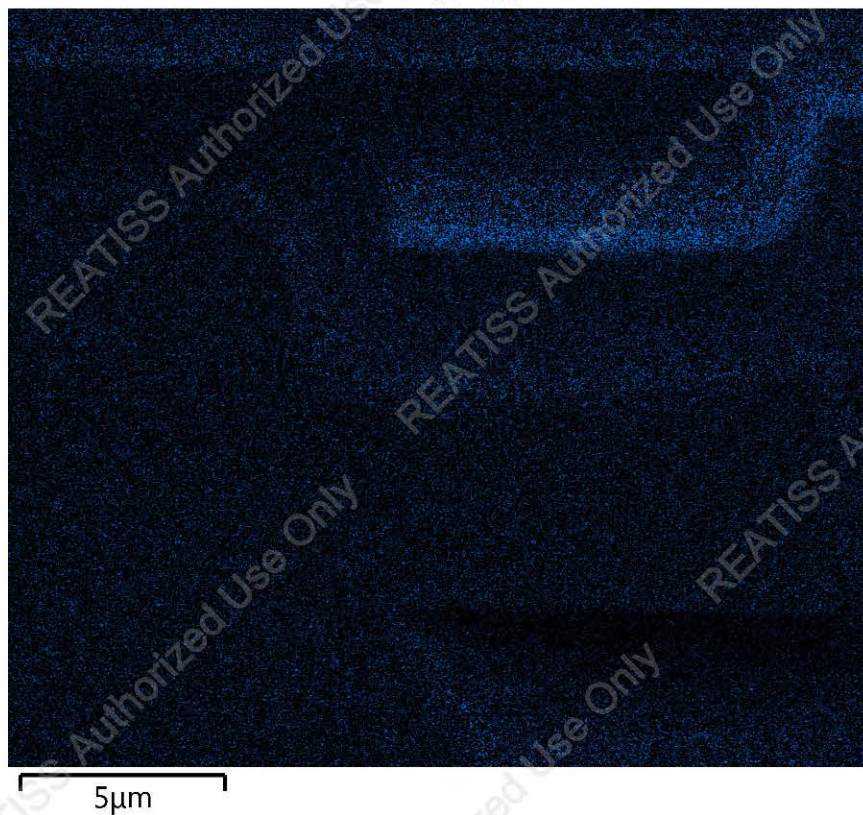


Figure 69. Nitrogen EDX map layer

Si K series

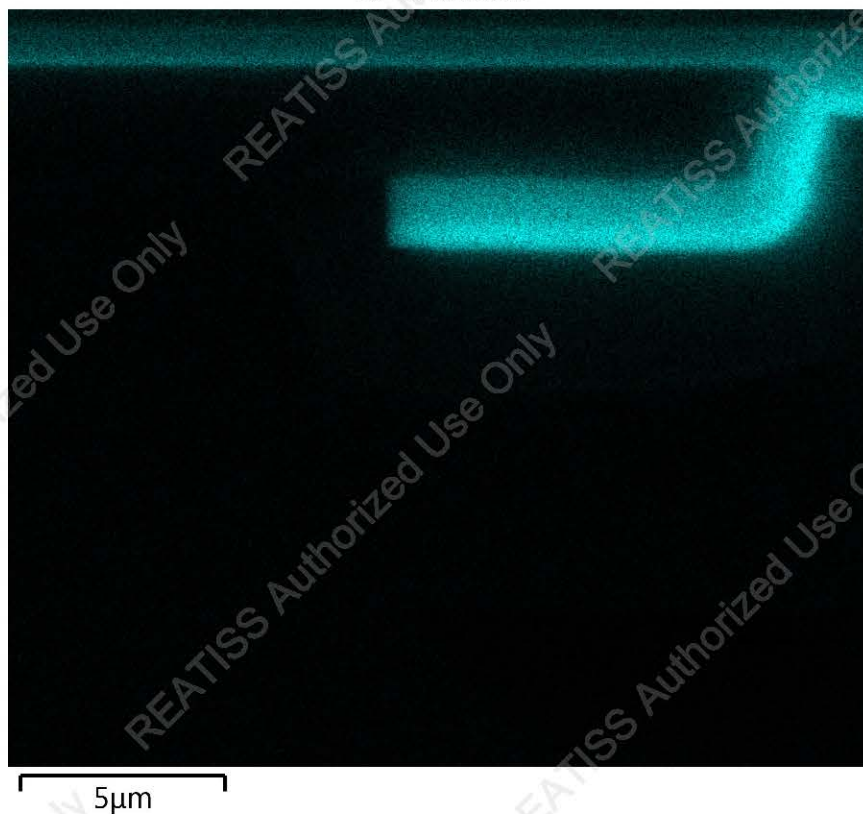


Figure 70. Silicon EDX map layer

O K series



Figure 71. Oxygen EDX map layer

C K series

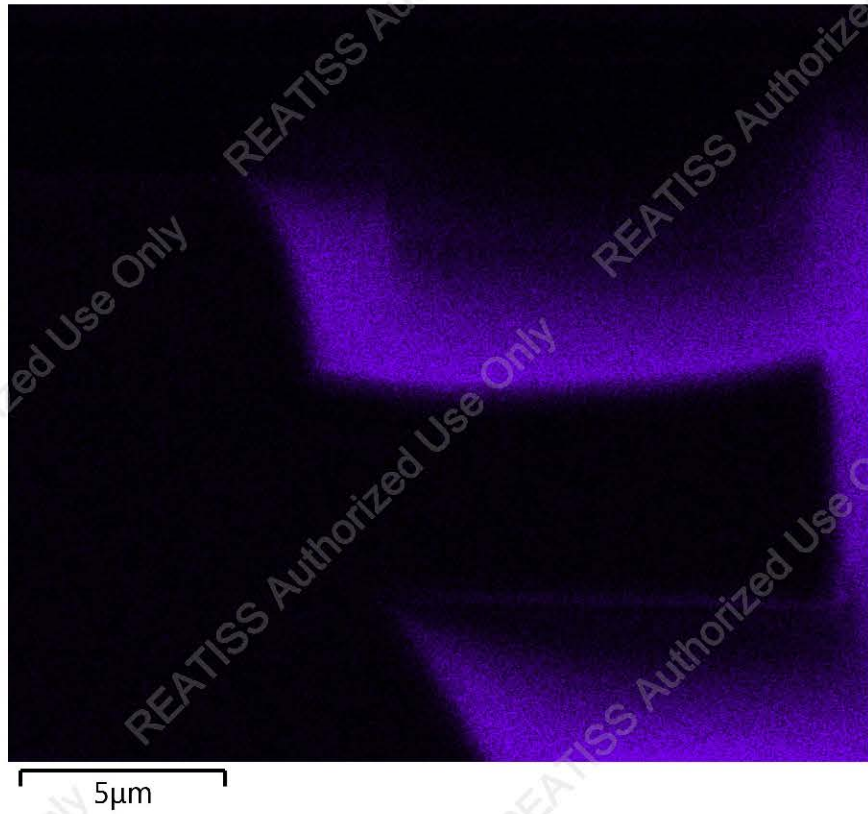


Figure 72. Carbon EDX map layer

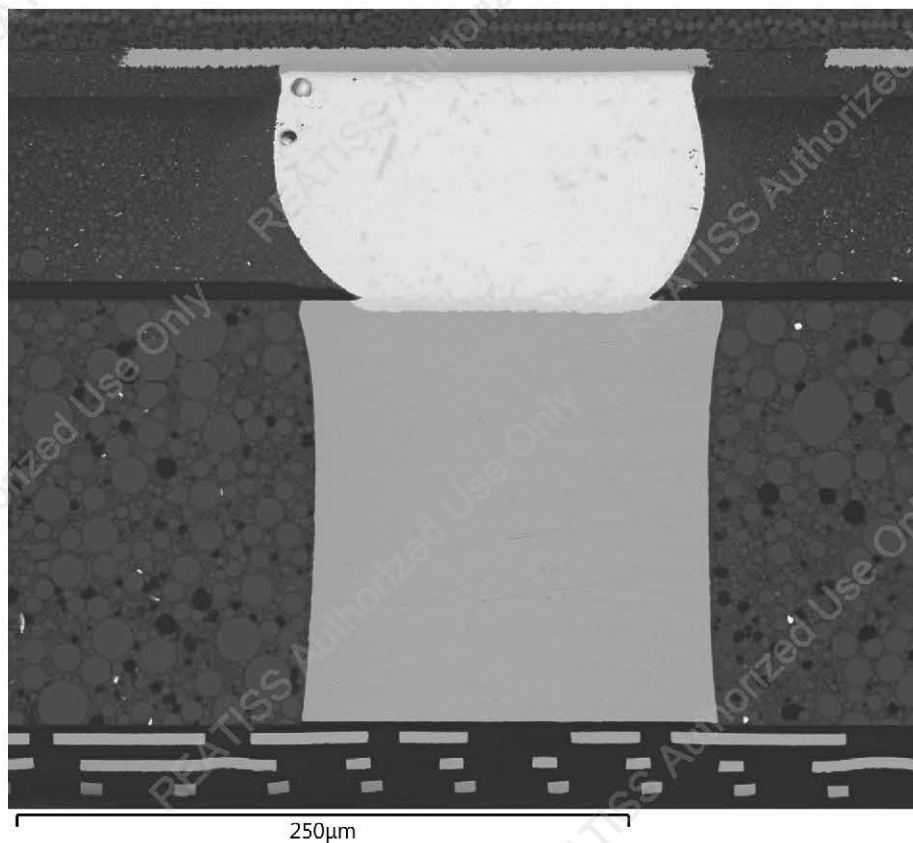


Figure 73. Package connection solder ball and TMV

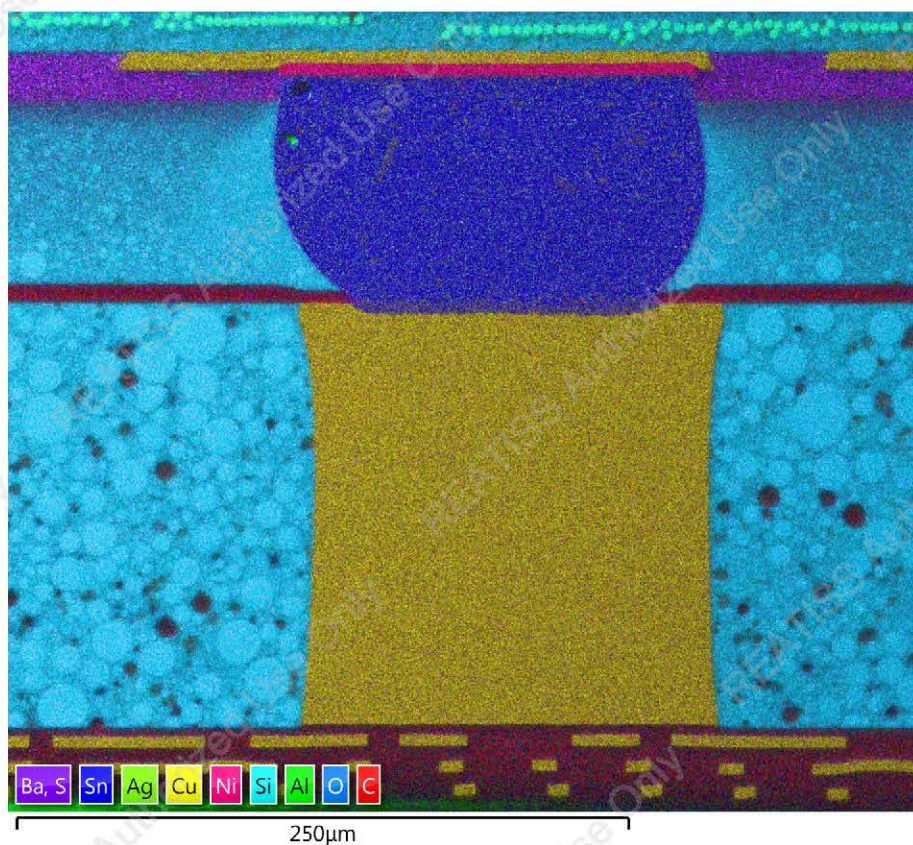


Figure 74. Layered EDX map of package connection solder ball and TMV

Sn L series

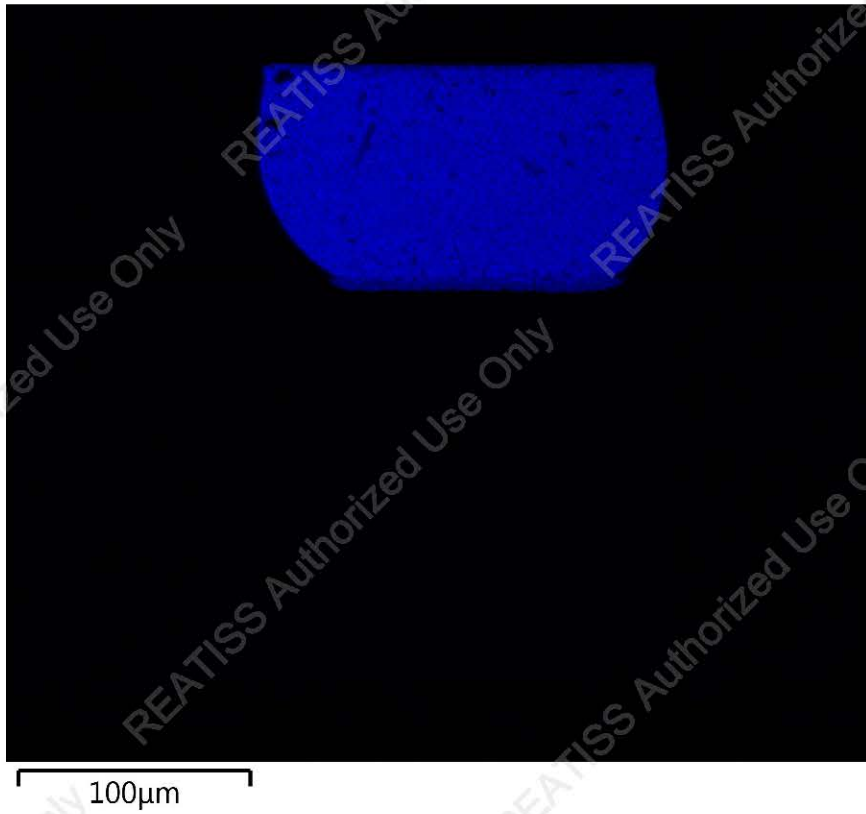


Figure 75. Tin EDX map layer

Cu K series

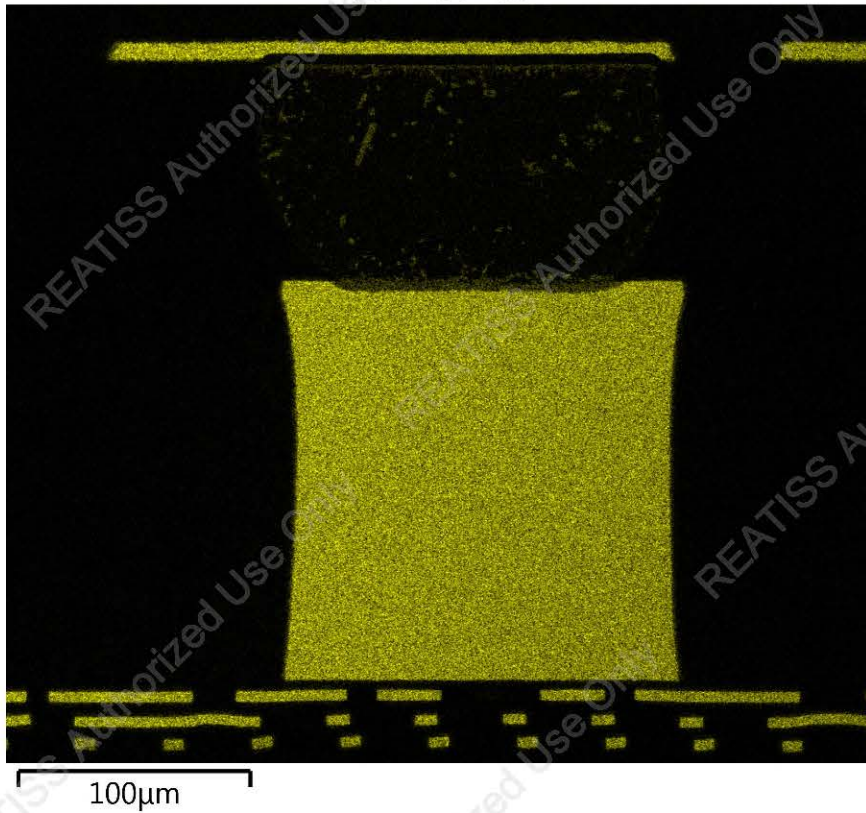


Figure 76. Copper EDX map layer

Al K series



Figure 77. Aluminum EDX map layer

Ni K series

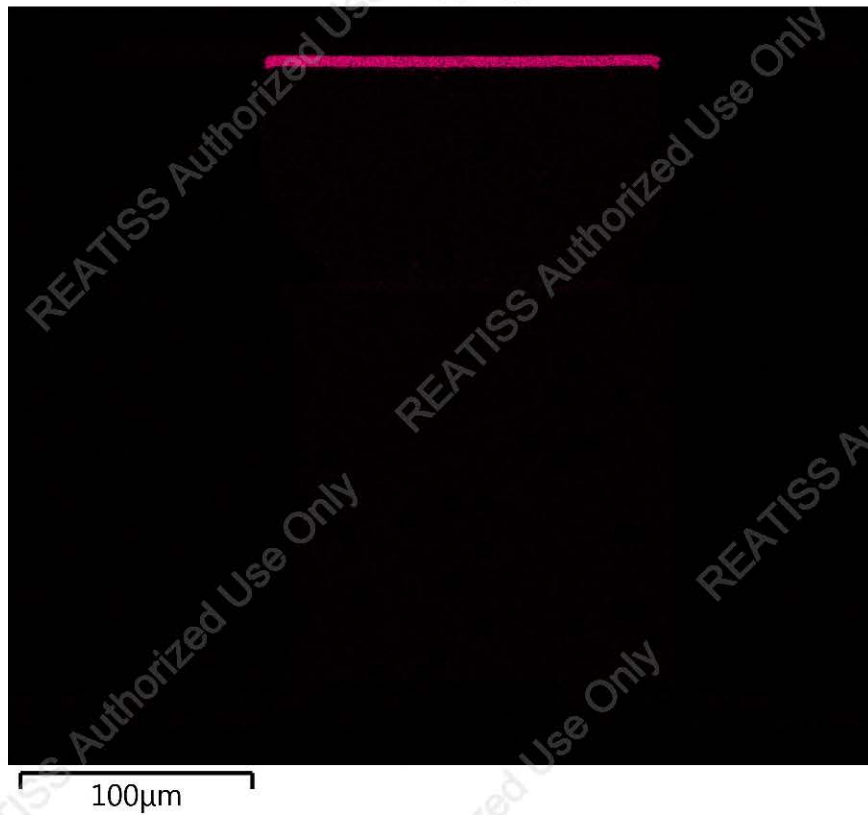


Figure 78. Nickel EDX map layer

Ag L series

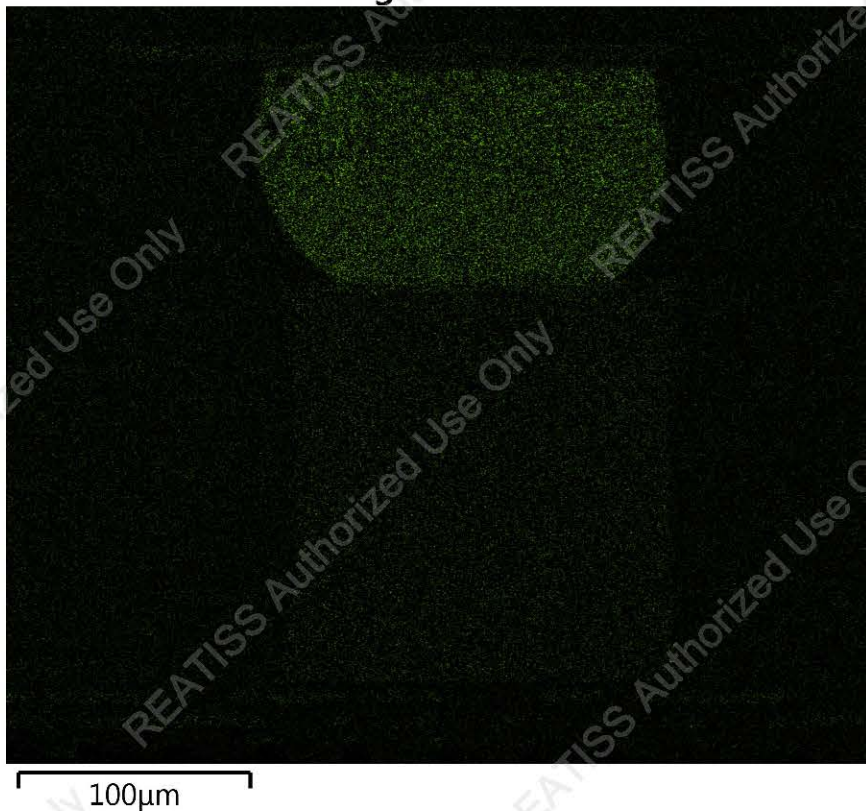


Figure 79. Silver EDX map layer

Si K series

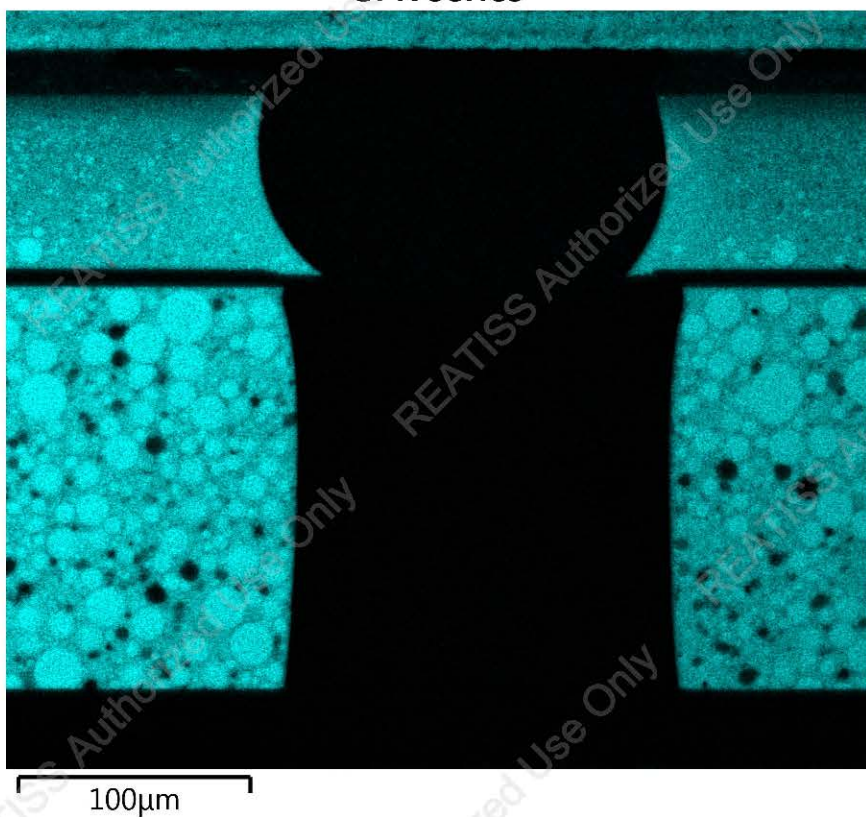


Figure 80. Silicon EDX map layer

O K series

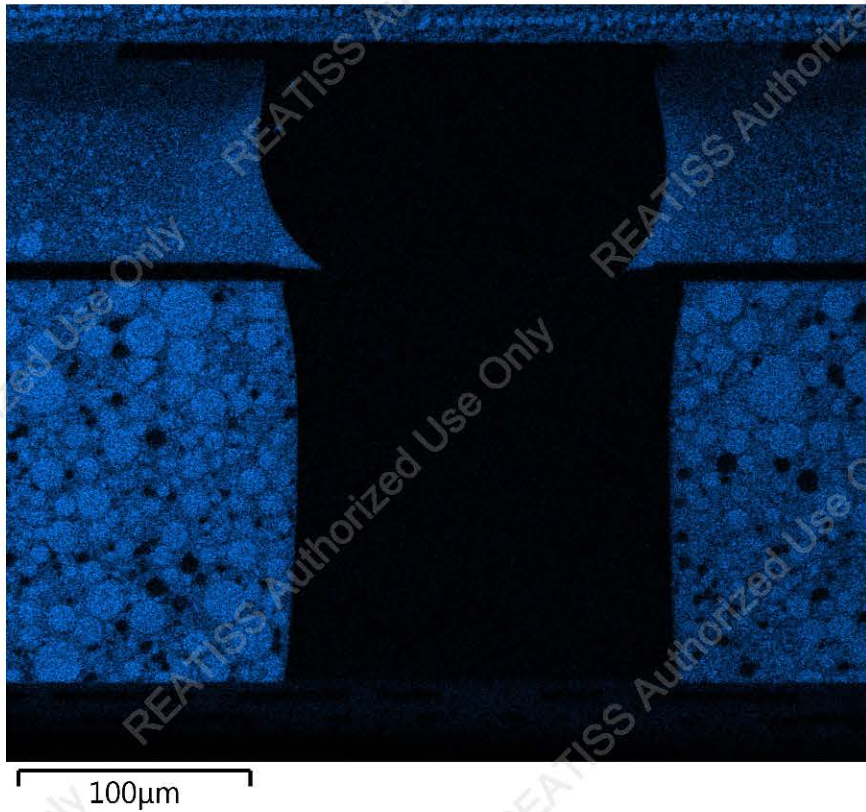


Figure 81. Oxygen EDX map layer

C K series

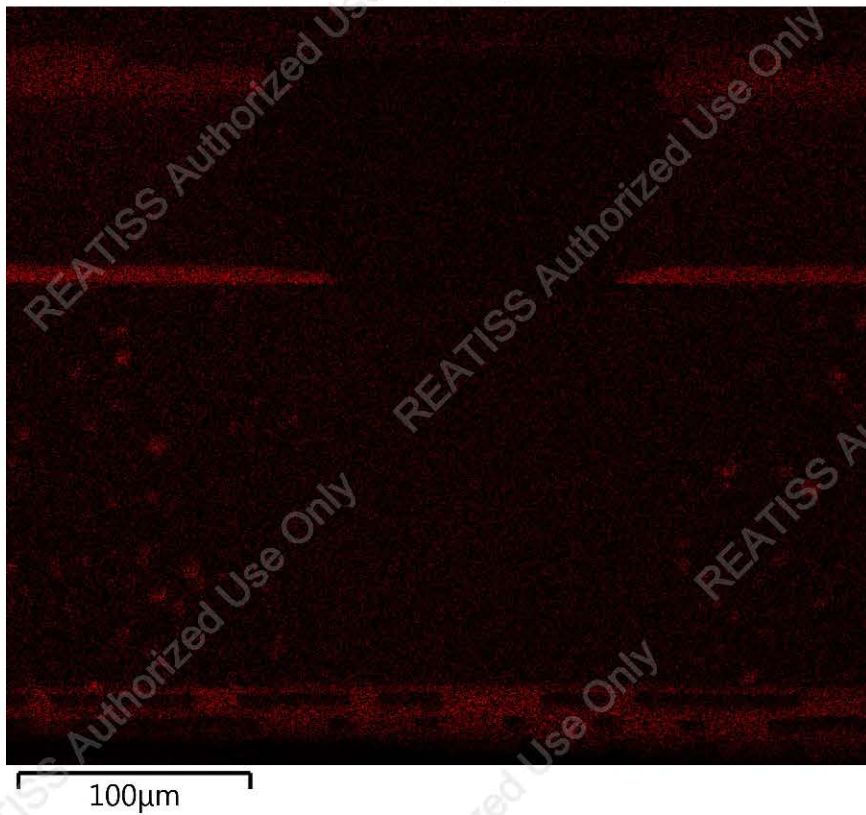


Figure 82. Carbon EDX map layer

Ba L series

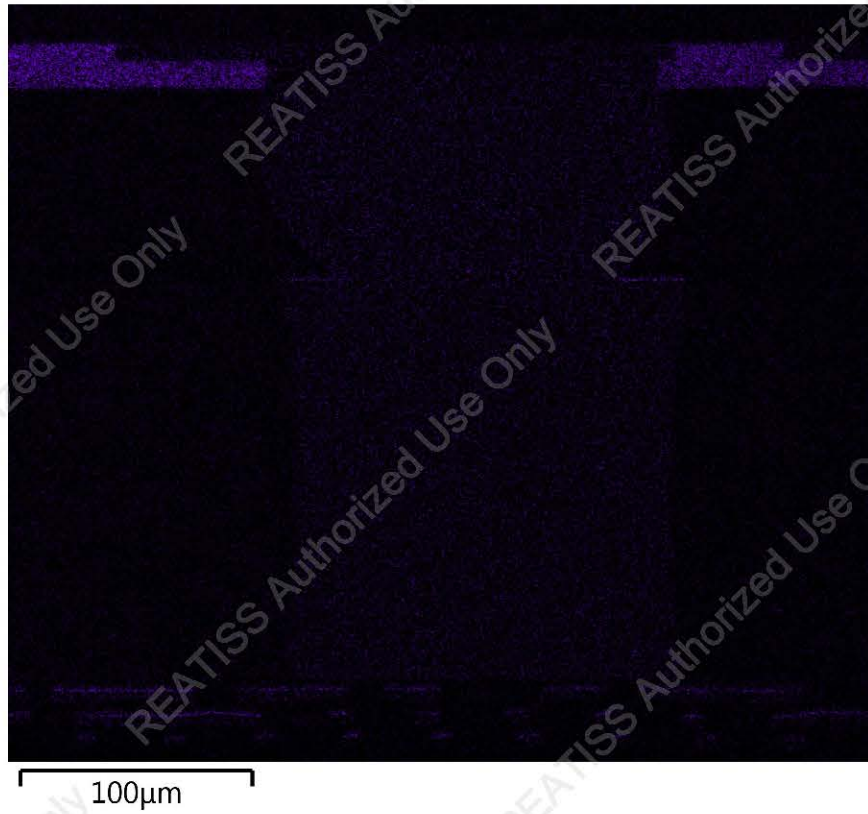


Figure 83. Barium EDX map layer

S K series

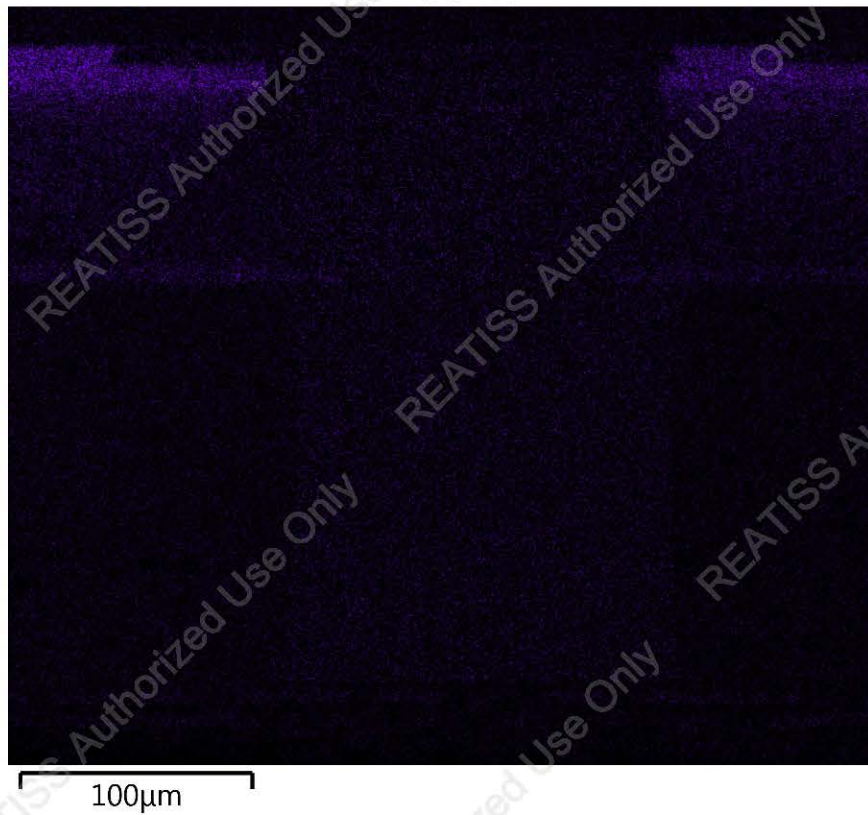


Figure 84. Sulfur EDX map layer

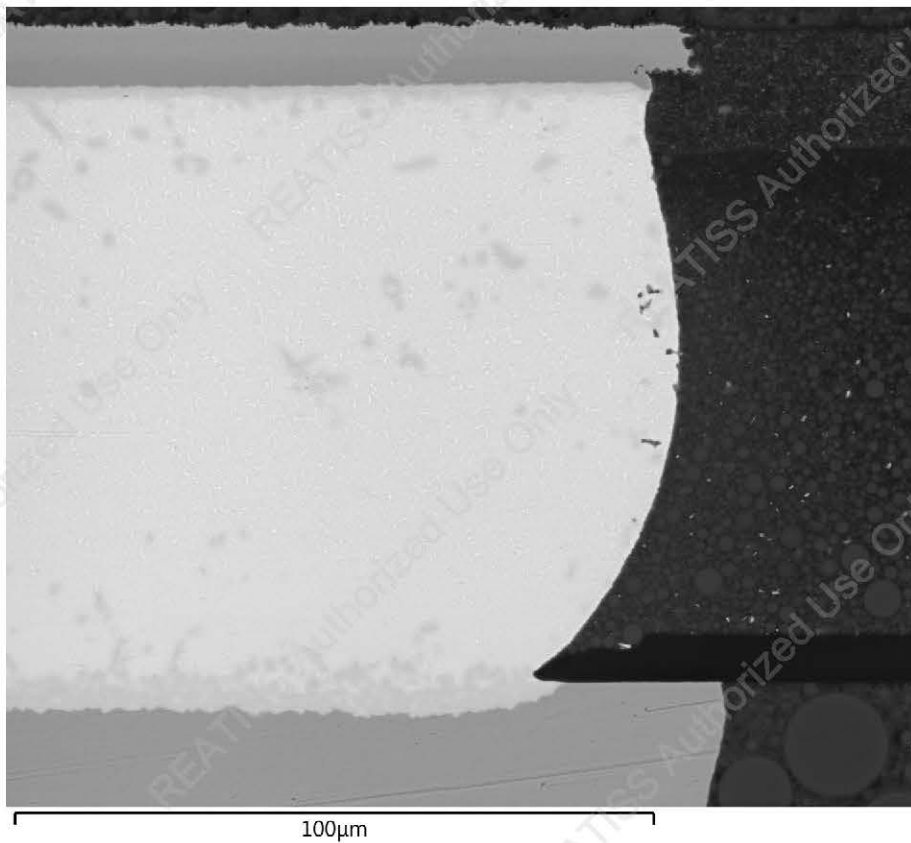


Figure 85. Package connection solder ball edge

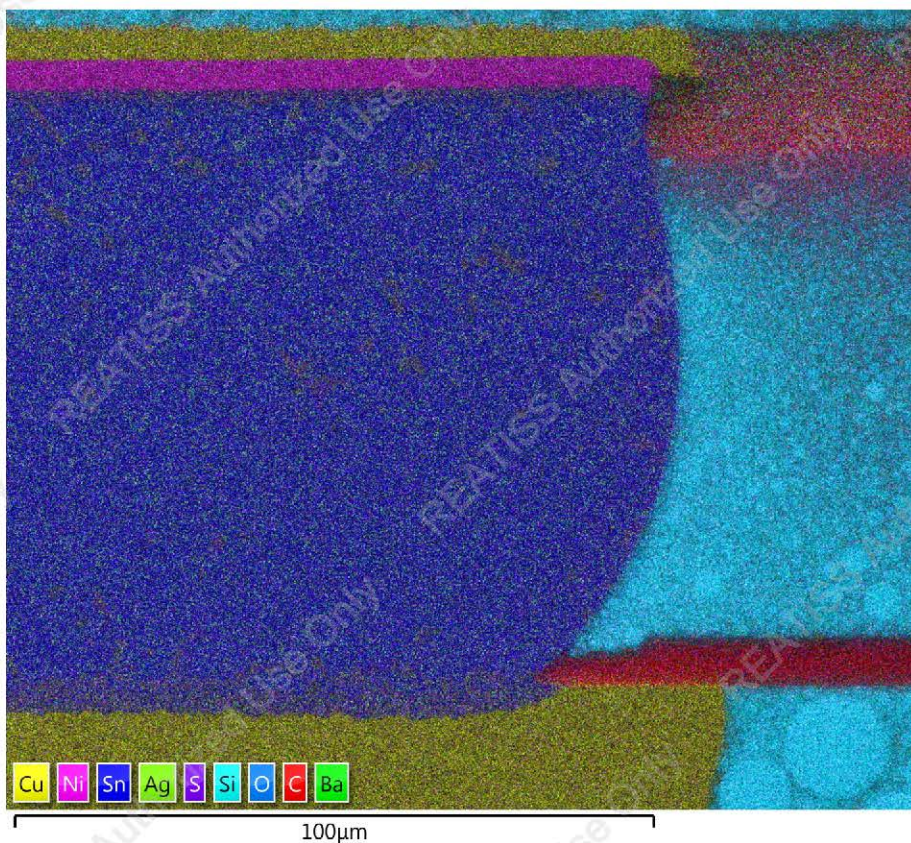


Figure 86. Layered EDX map of package connection solder ball edge

Sn L series

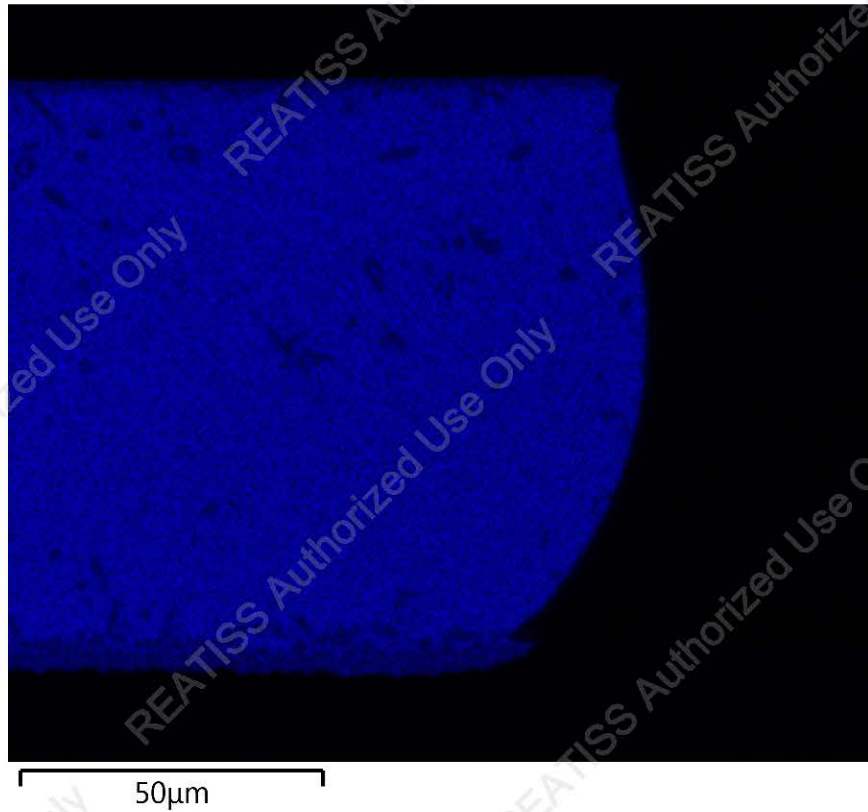


Figure 87. Tin EDX map layer

Cu K series

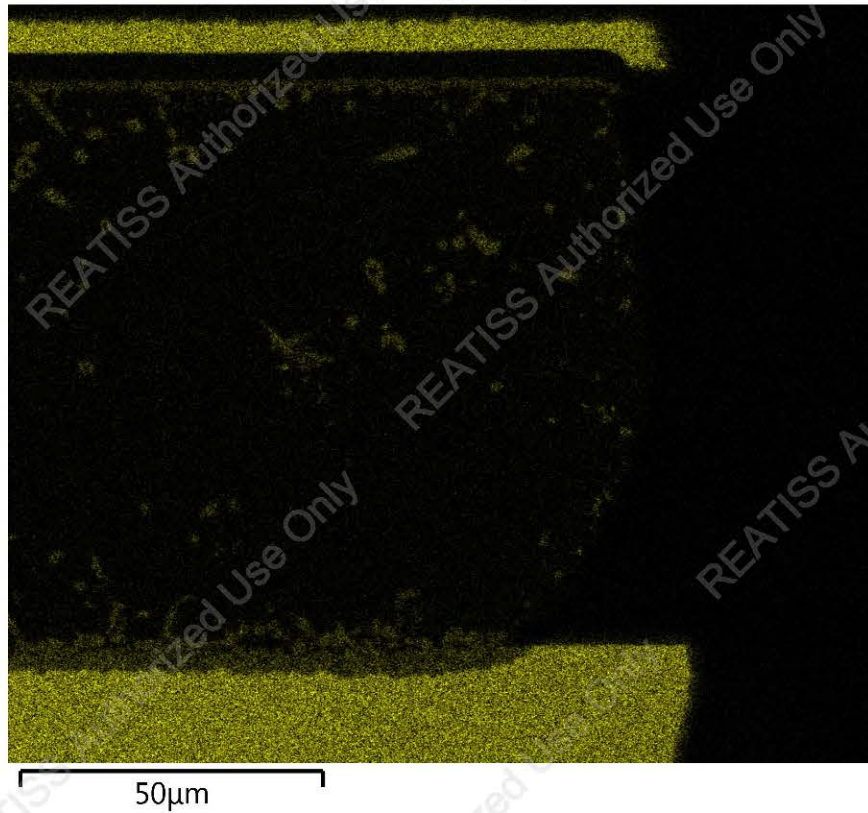


Figure 88. Copper EDX map layer

Ni K series

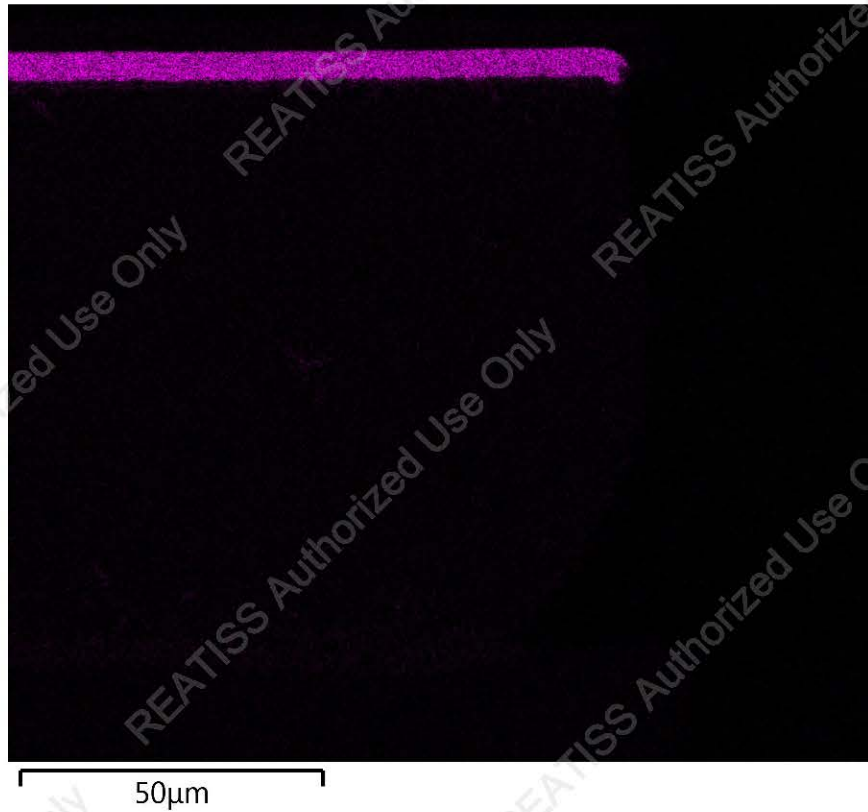


Figure 89. Nickel EDX map layer

Ag L series

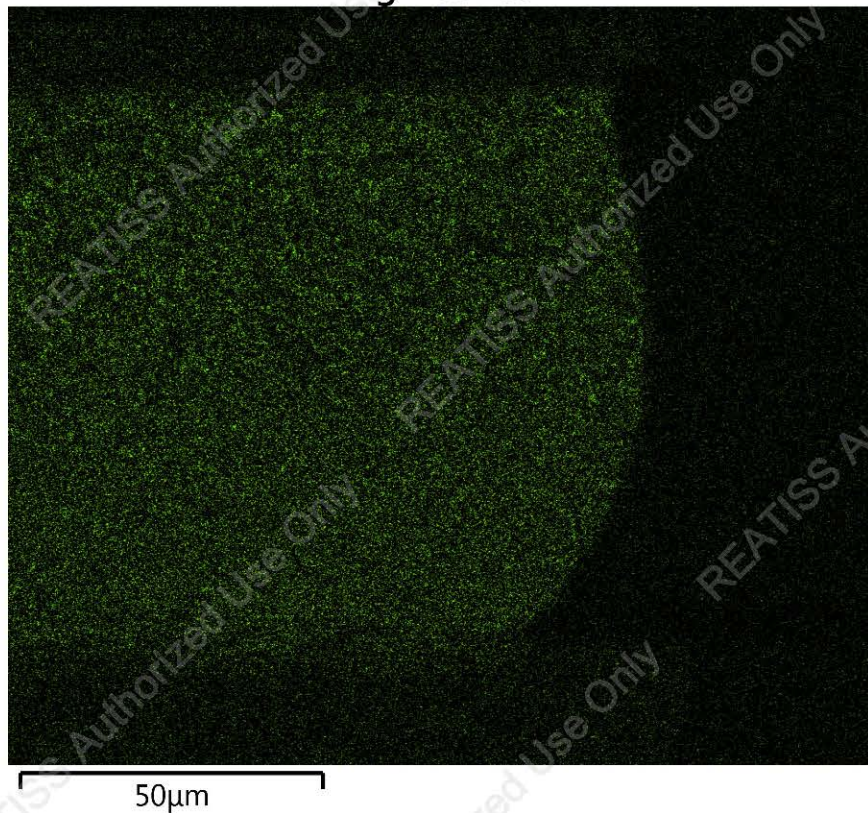


Figure 90. Silver EDX map layer

Si K series

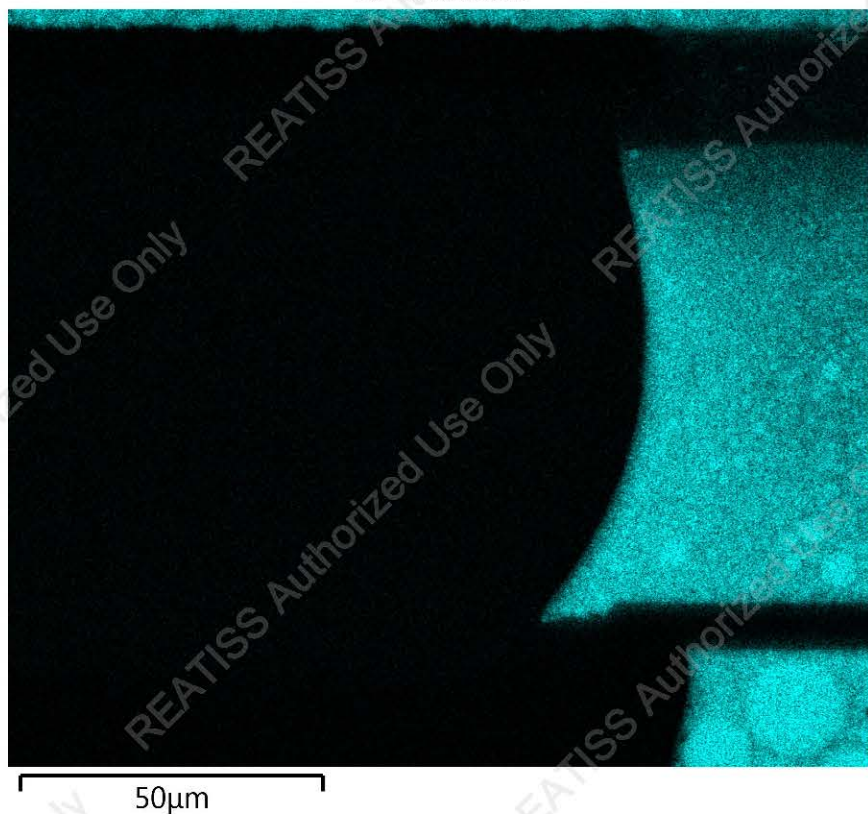


Figure 91. Silicon EDX map layer

O K series

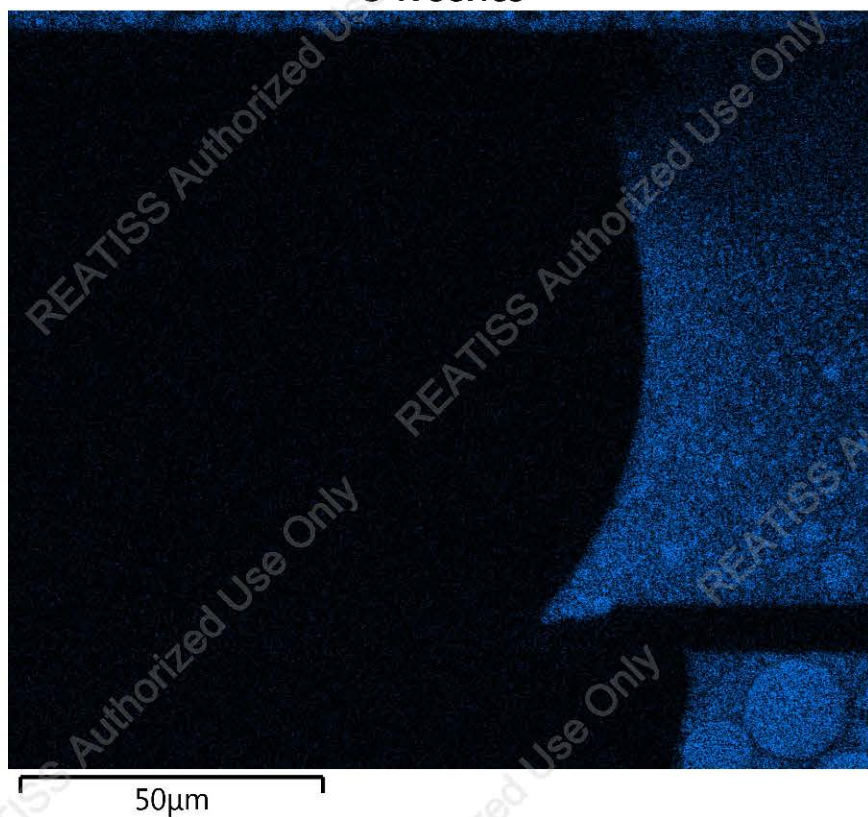


Figure 92. Oxygen EDX map layer

C K series

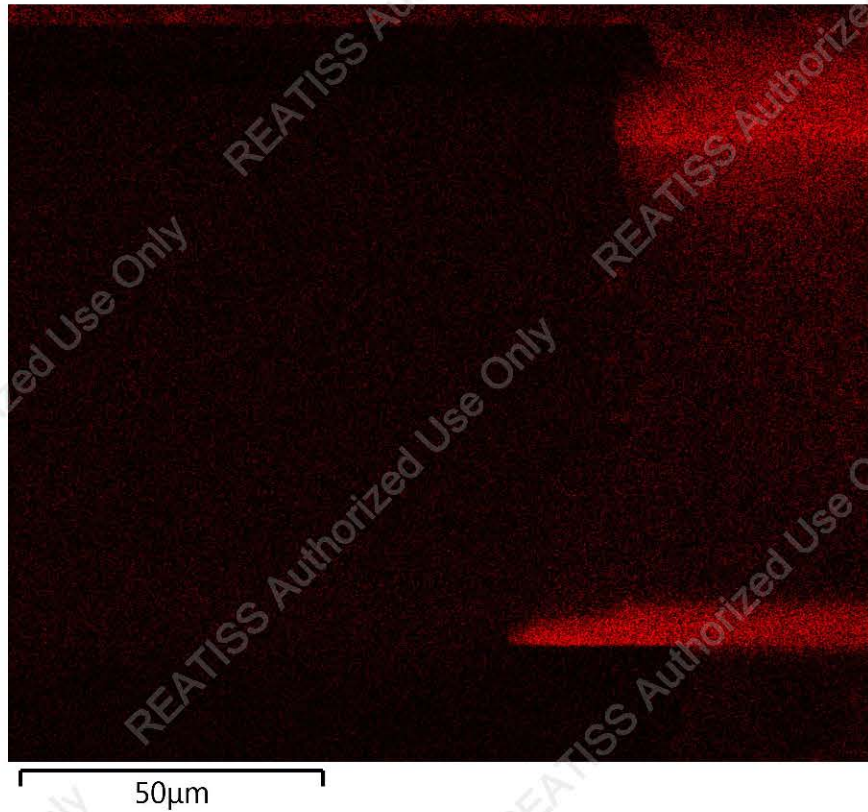


Figure 93. Carbon EDX map layer

Ba L series

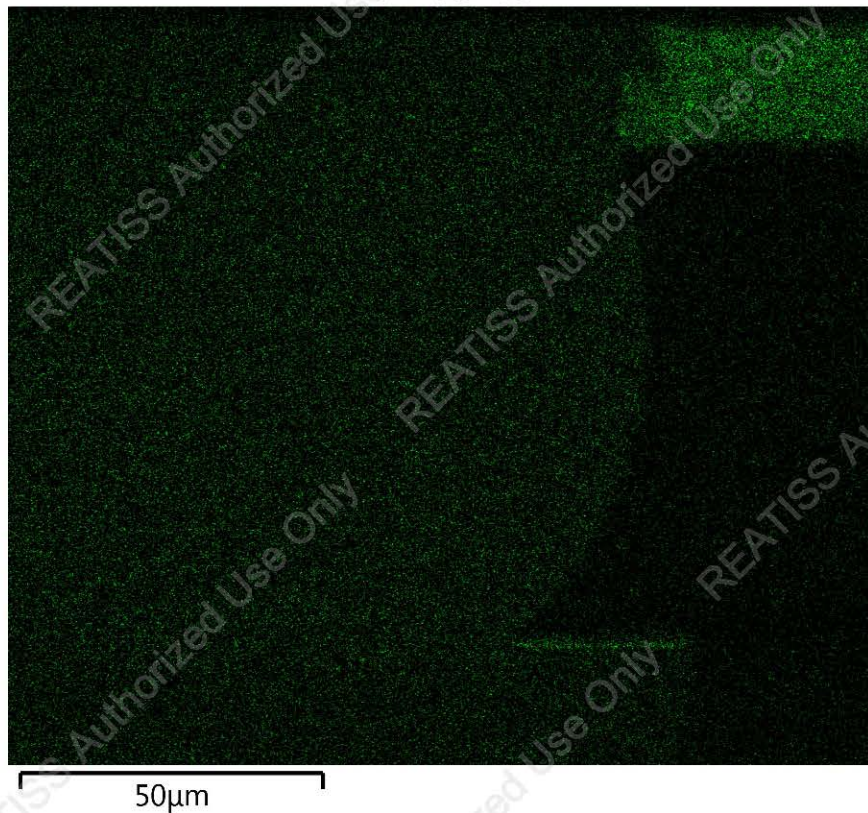


Figure 94. Barium EDX map layer

S K series

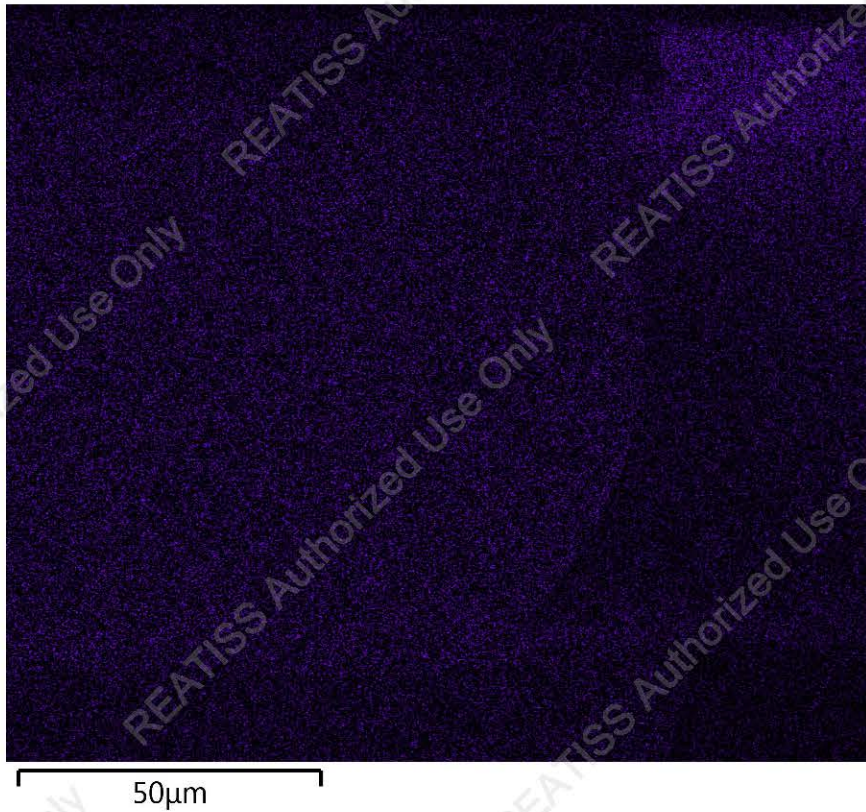


Figure 95. Sulfur EDX map layer