Apple [redacted]
Application Processor

Package Analysis Report

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Device Summary Sheet

Manufacturer:	Apple Inc.
Part Number:	[redacted]
Date Code:	Not identified
IC Type:	64-bit quad-core SoC

Technology synopsis

Package Type:	BGA
Pin Count:	1407
Package Size:	14,4 mm x 15,8 mm x 0,9 mm
Die Count:	3. One [redacted] processor die and two Micron LPDDR4 memory dice
[redacted] **Die Size:**	10,92 mm x 11,53 mm (by edge of physical silicon) 10,9 mm x 11,34 mm (by edge of seal)
Micron LPDDR4 Die Size:	12,88 mm x 6,92 mm (by edge of physical silicon) 12,82 mm x 6,86 mm (by edge of seal)
[redacted] **Die Thickness [1] :**	162 µm
Micron LPDDR4 Die Thickness [1]:	108 µm
Processor Package Substrate Thickness [1]:	39 µm
Memory Package Substrate Thickness [1]:	87 µm

[1] Measured feature sizes are accurate within 2%

Source Device

Figure 1. Apple [redacted] iPhone [redacted] front side

Figure 2. Apple [redacted] iPhone [redacted] back side

Figure 3. Apple [redacted] iPhone [redacted] main PCB side A

Apple [redacted]

Figure 4. Apple [redacted] iPhone [redacted] main PCB side B

Die and Package

Figure 5. Package top

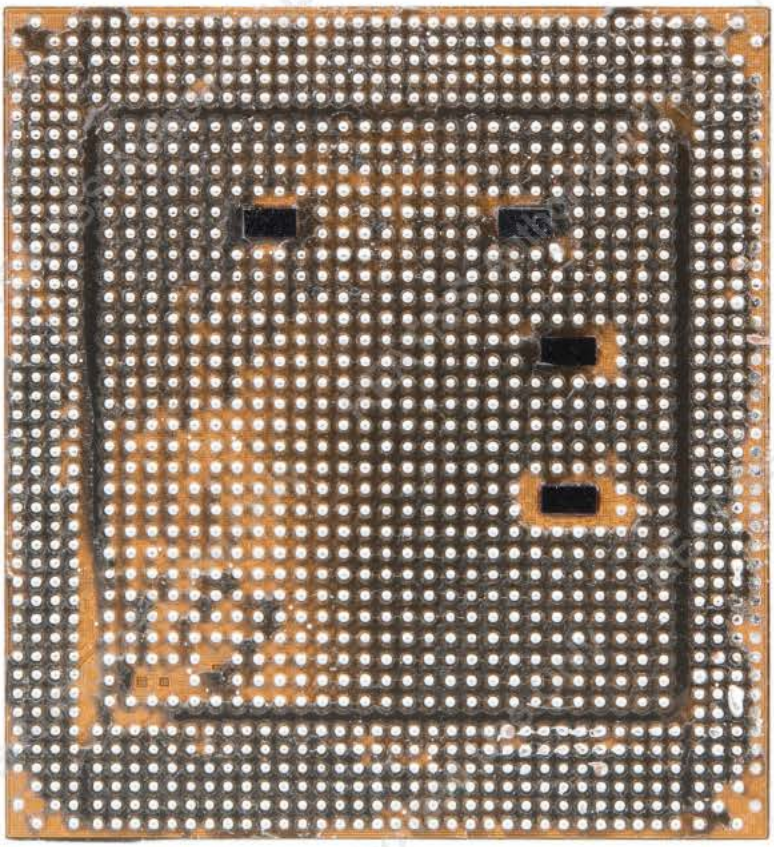


Figure 6. Package bottom

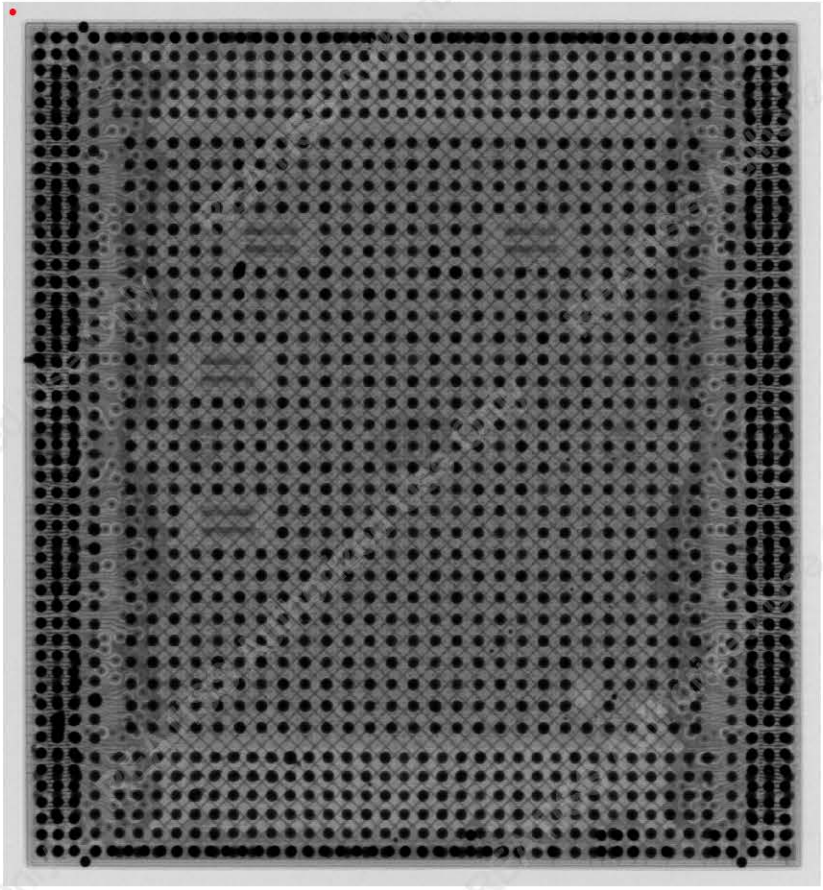


Figure 7. Package X-ray

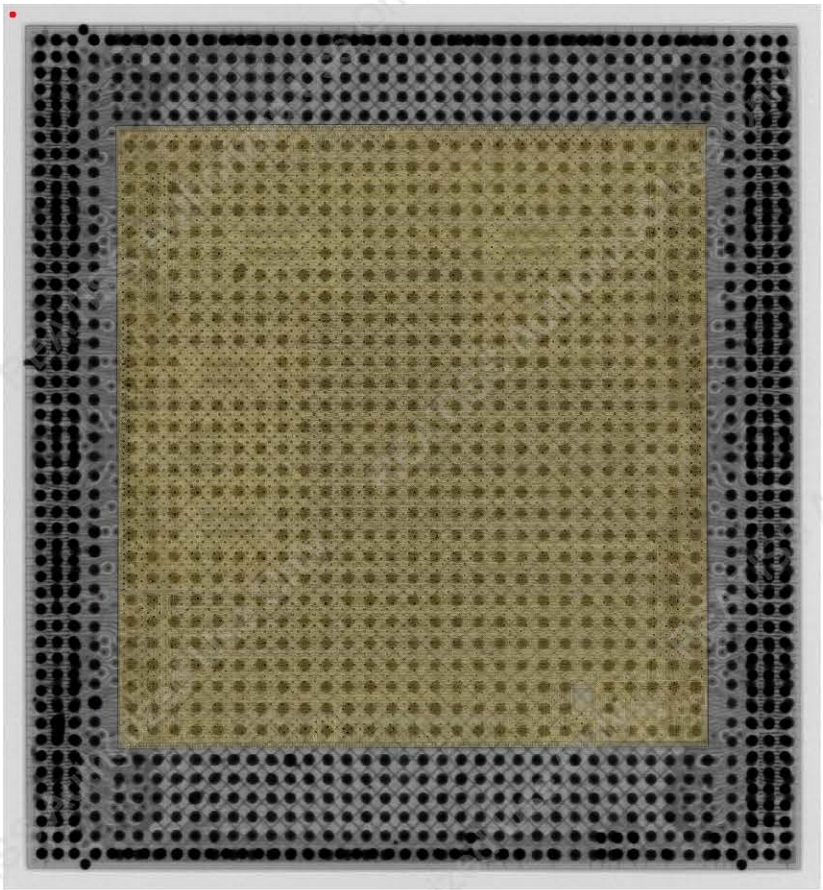


Figure 8. Package X-ray combined with [redacted] die photo

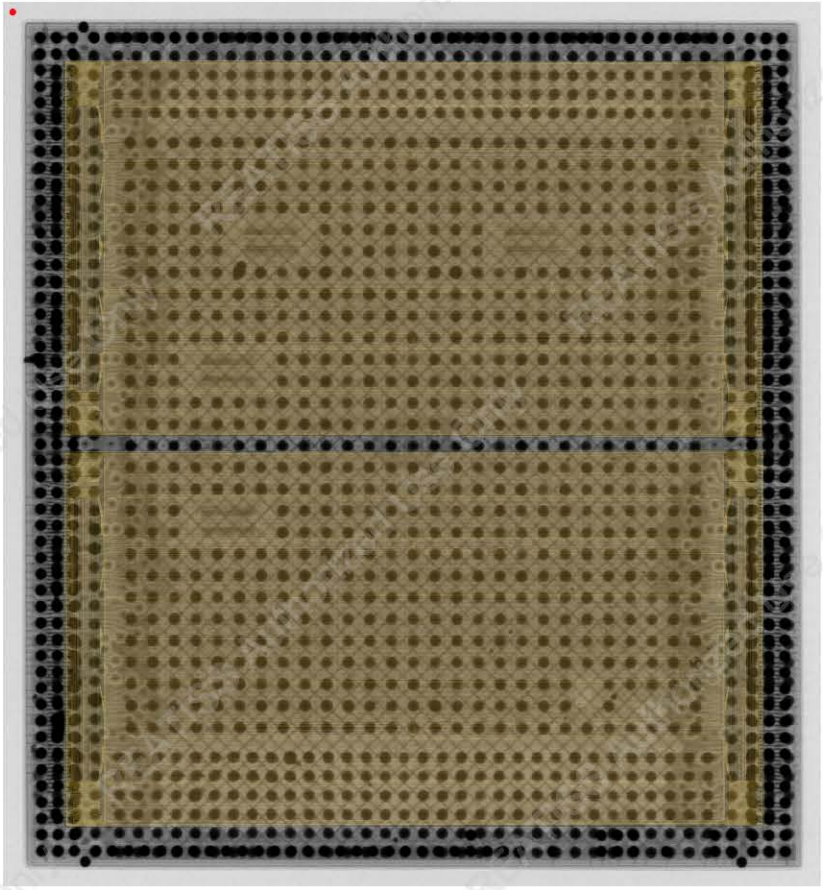


Figure 9. Package X-ray combined with Micron LPDDR4 dice photos

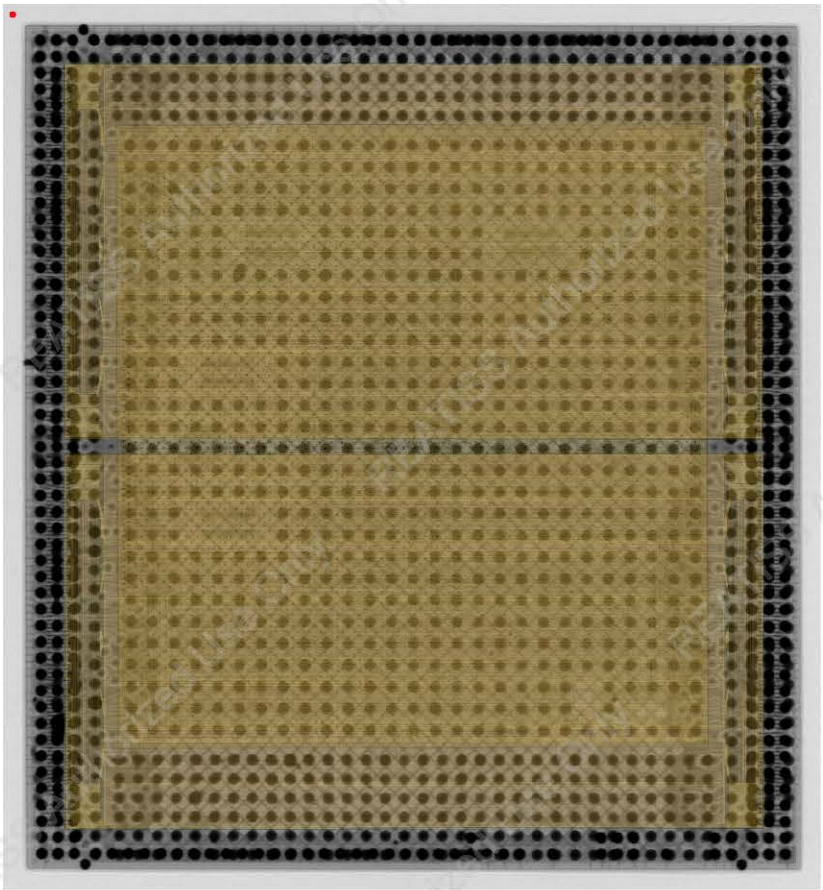


Figure 10. Package X-ray combined with dice photos

Figure 11. [redacted] die photo (top metal)

Figure 12. [redacted] die markings

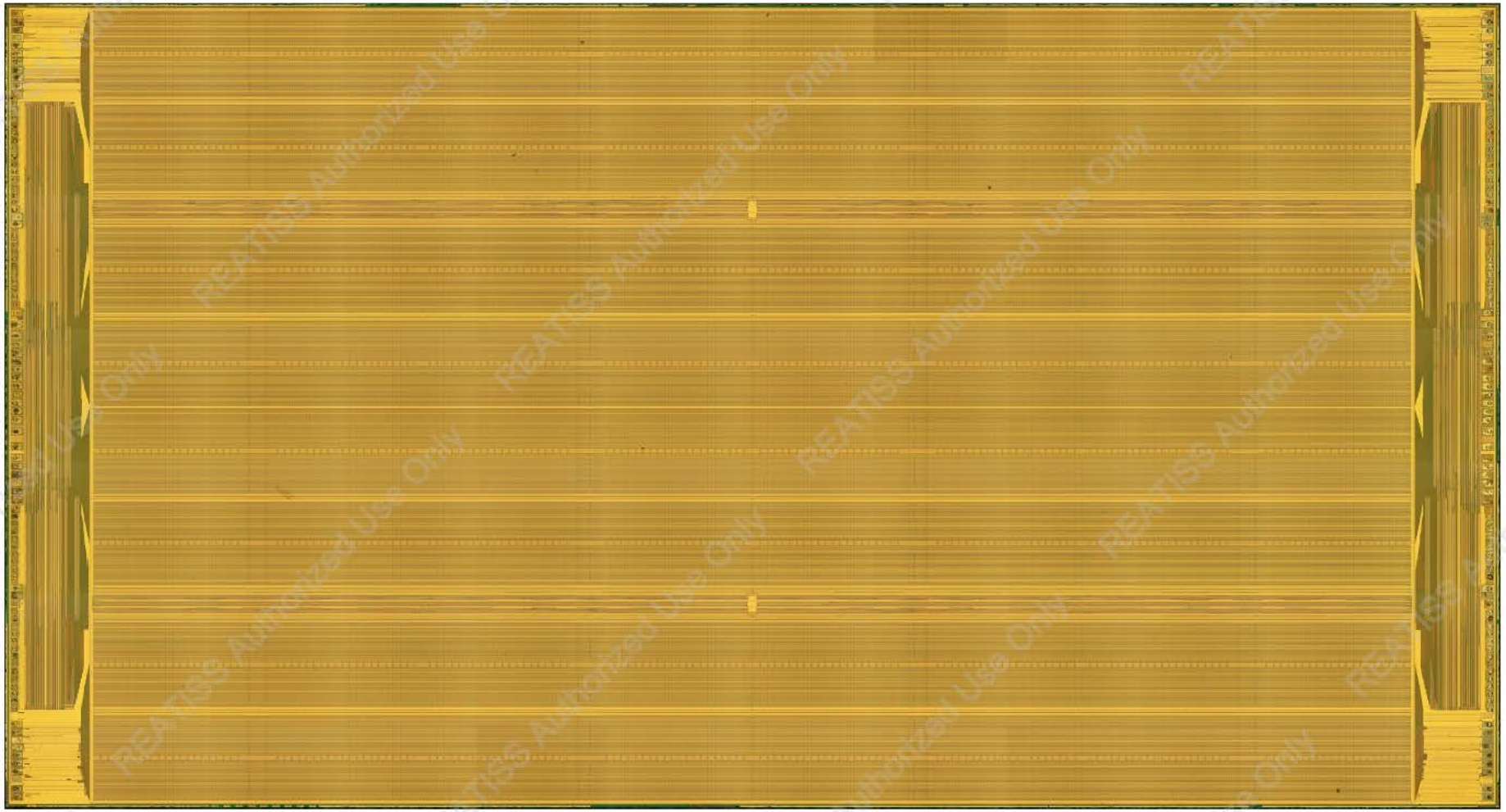


Figure 13. Micron LPDDR4 die photo (top metal)

Figure 14. Micron LPDDR4 die markings

Package Analysis

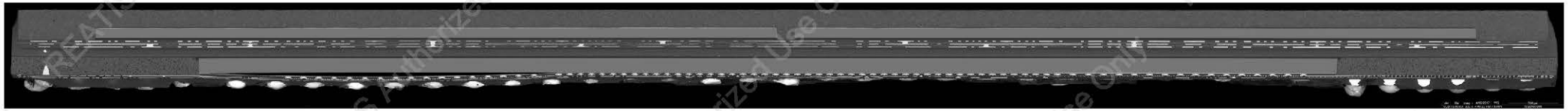
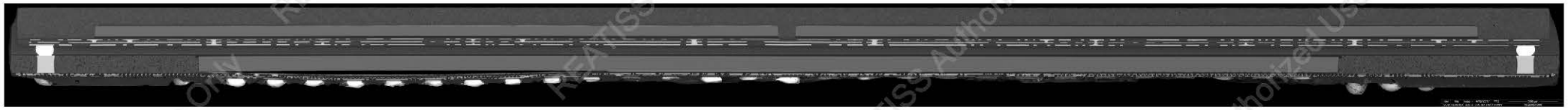


Figure 15. Package cross section



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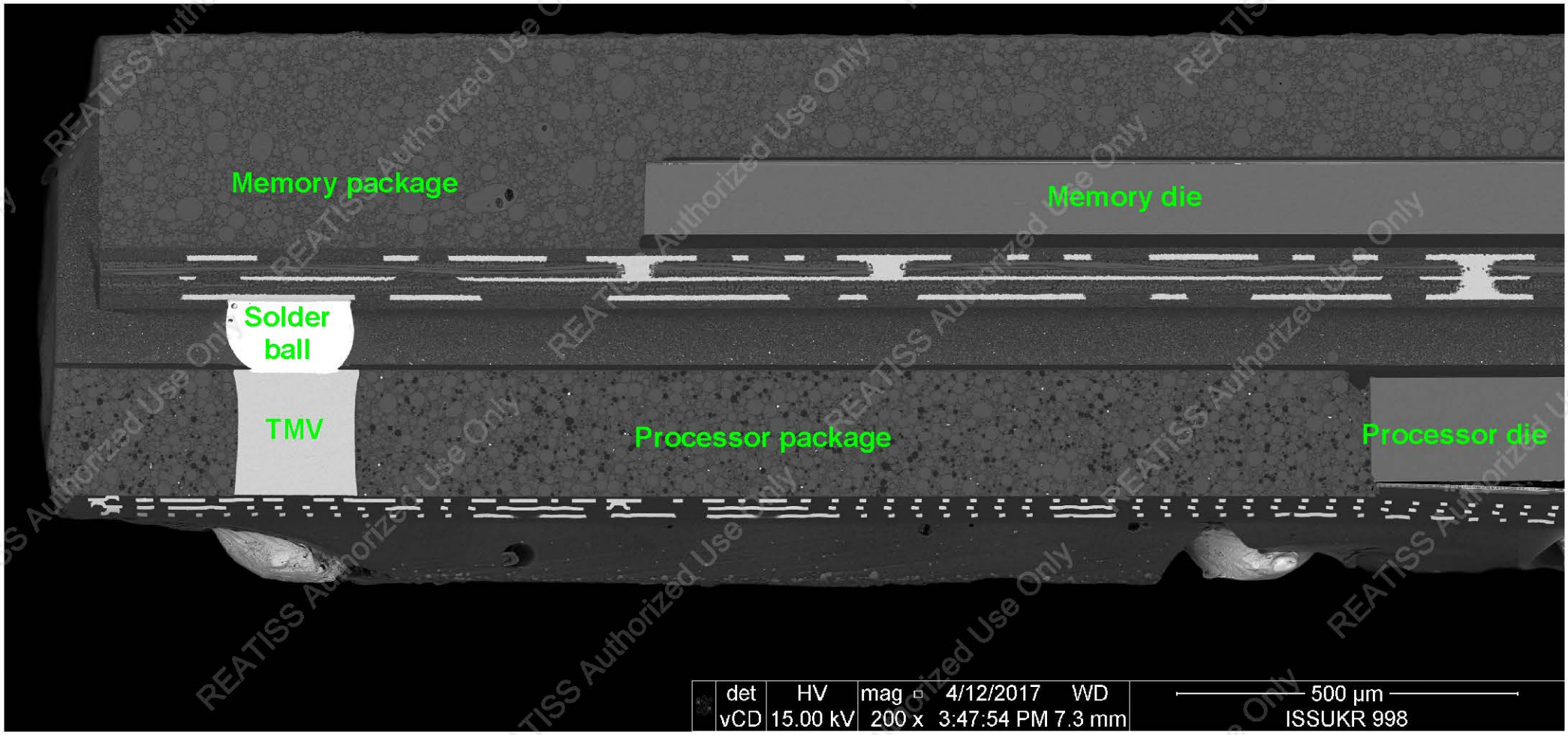


Figure 17. Package assembly left edge

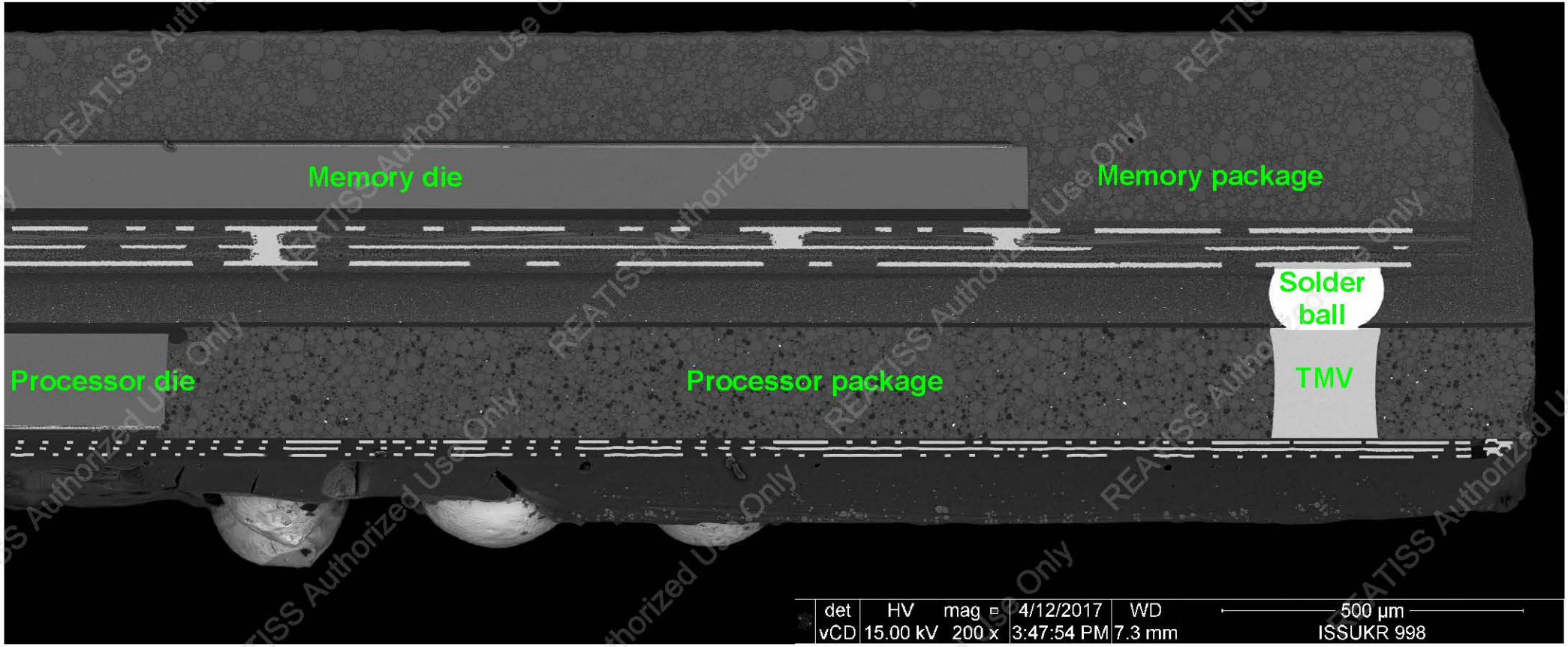


Figure 18. Package assembly right edge

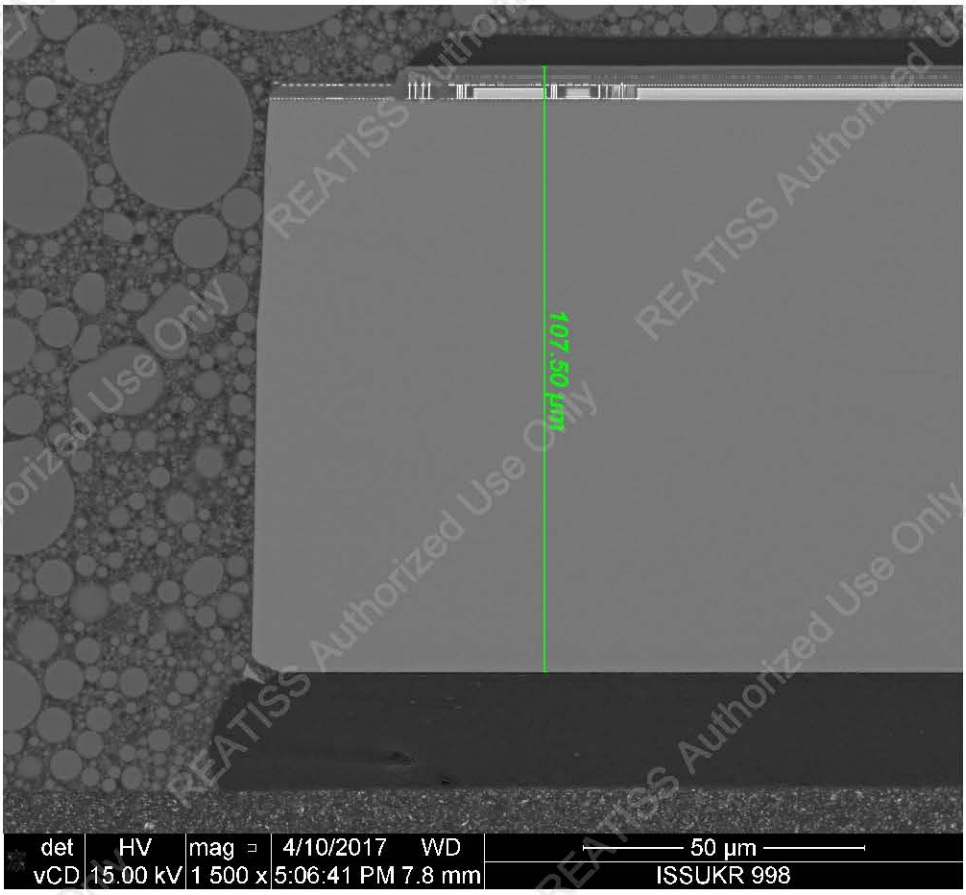


Figure 19. Memory die assembly

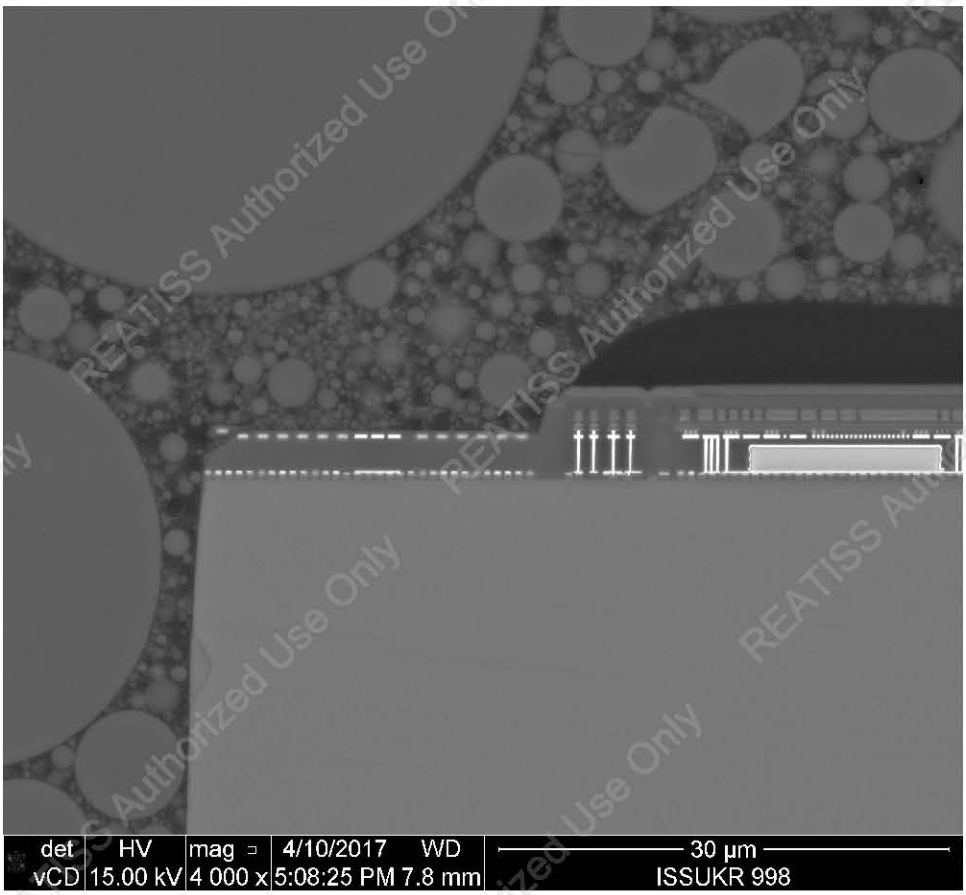


Figure 20. Memory die corner and encapsulation

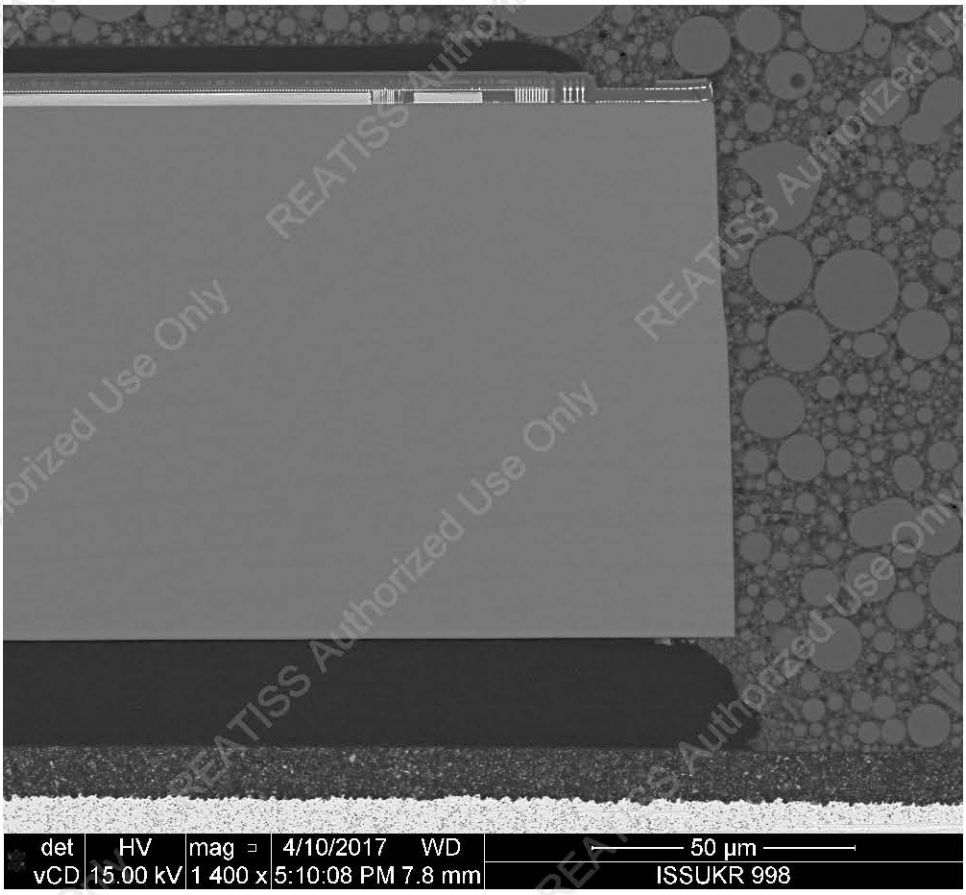


Figure 21. Memory die assembly

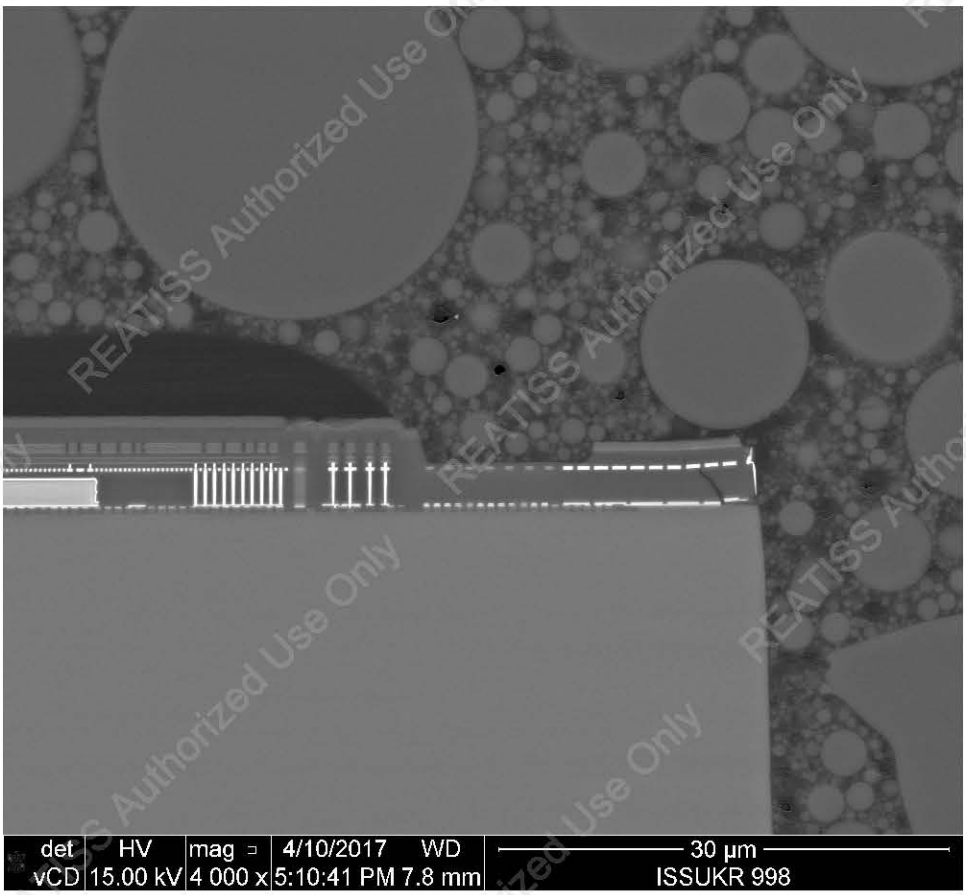


Figure 22. Memory die corner and encapsulation

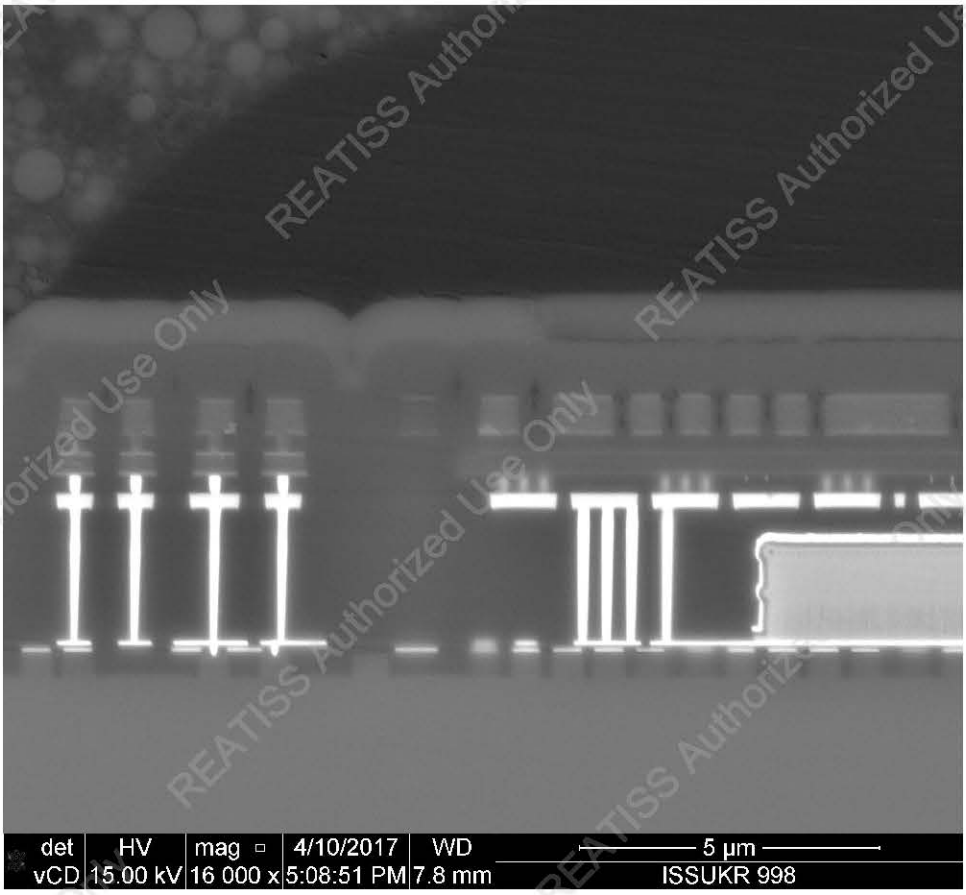
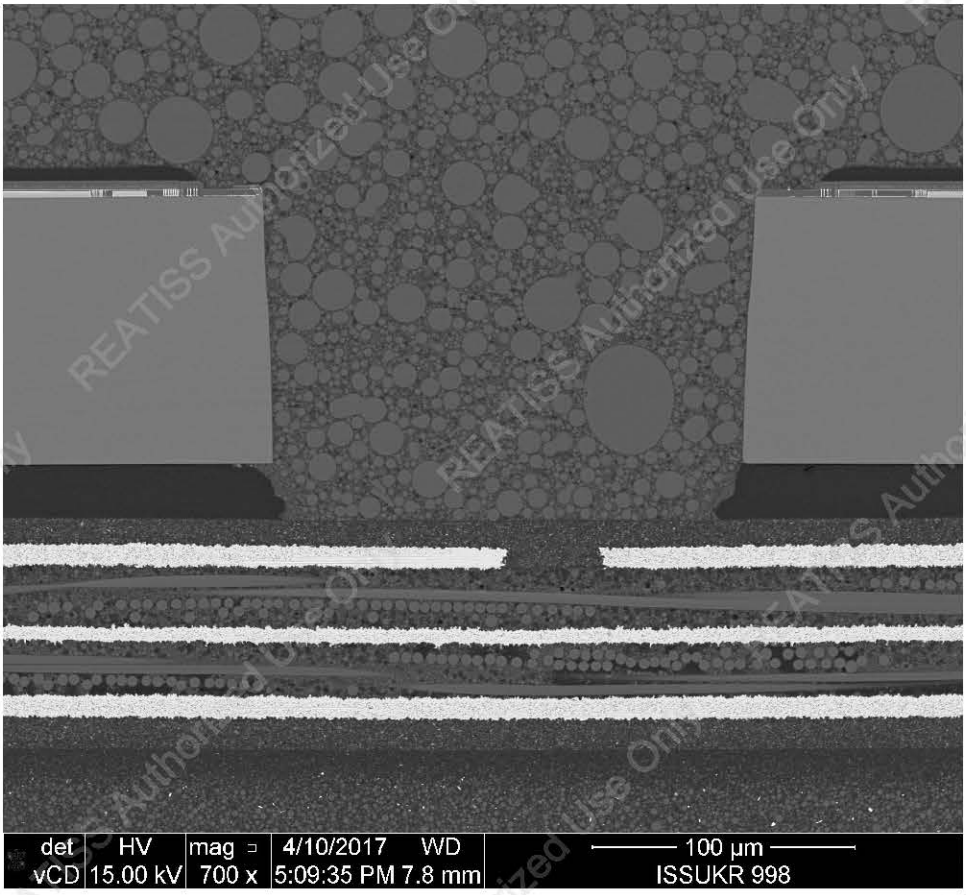


Figure 23. Memory die edge seal ring



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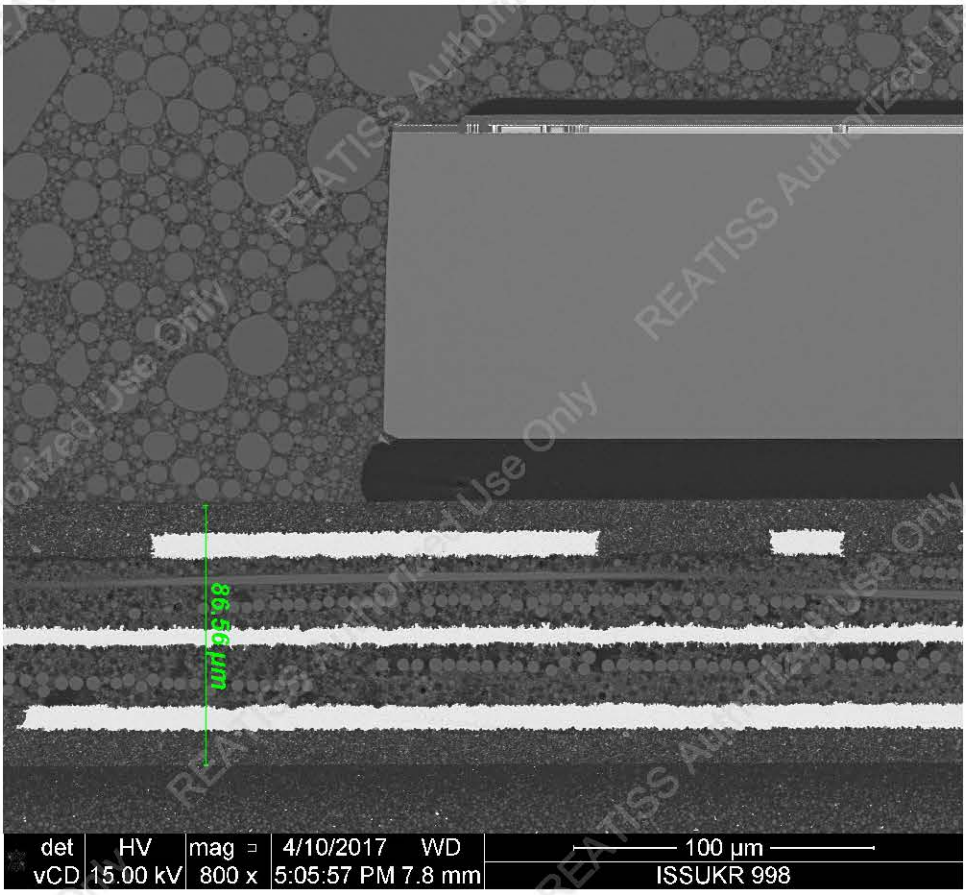
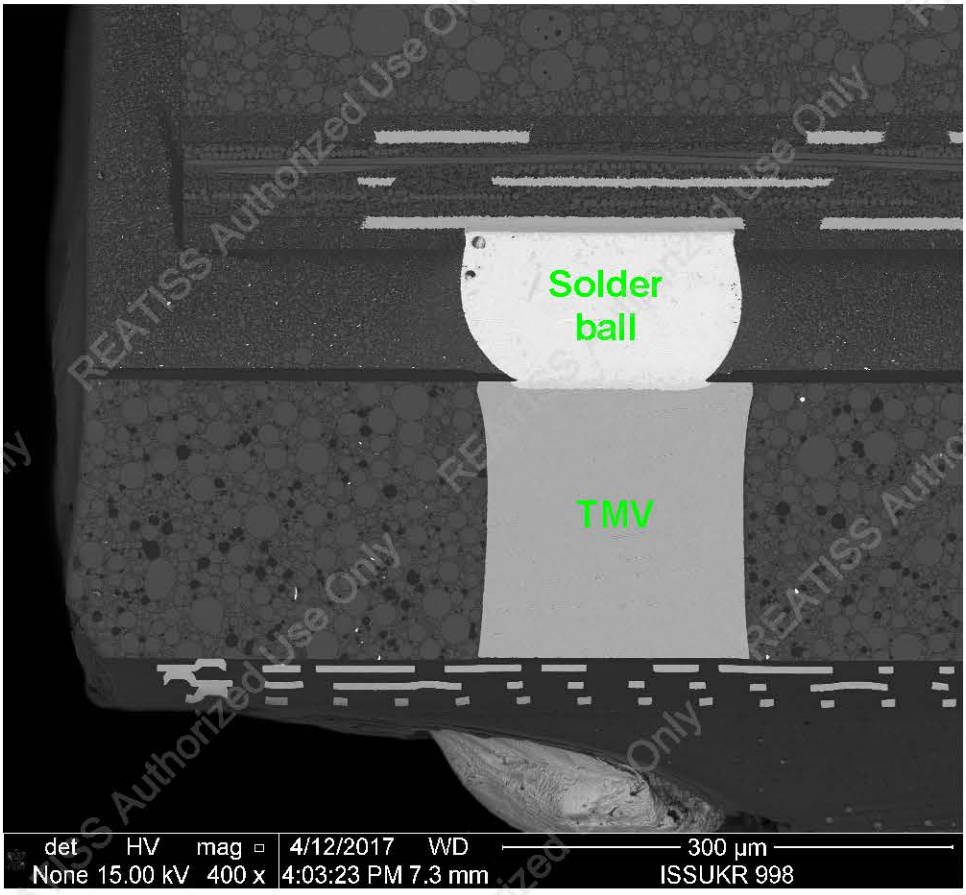


Figure 25. Memory package substrate



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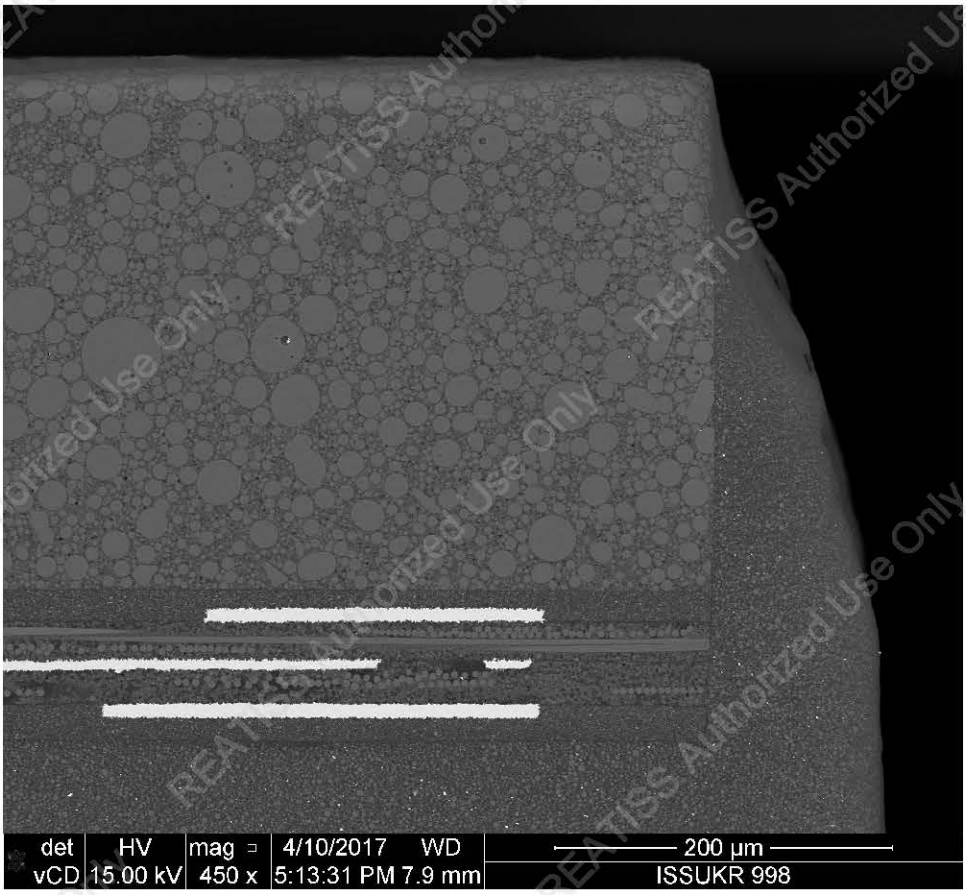

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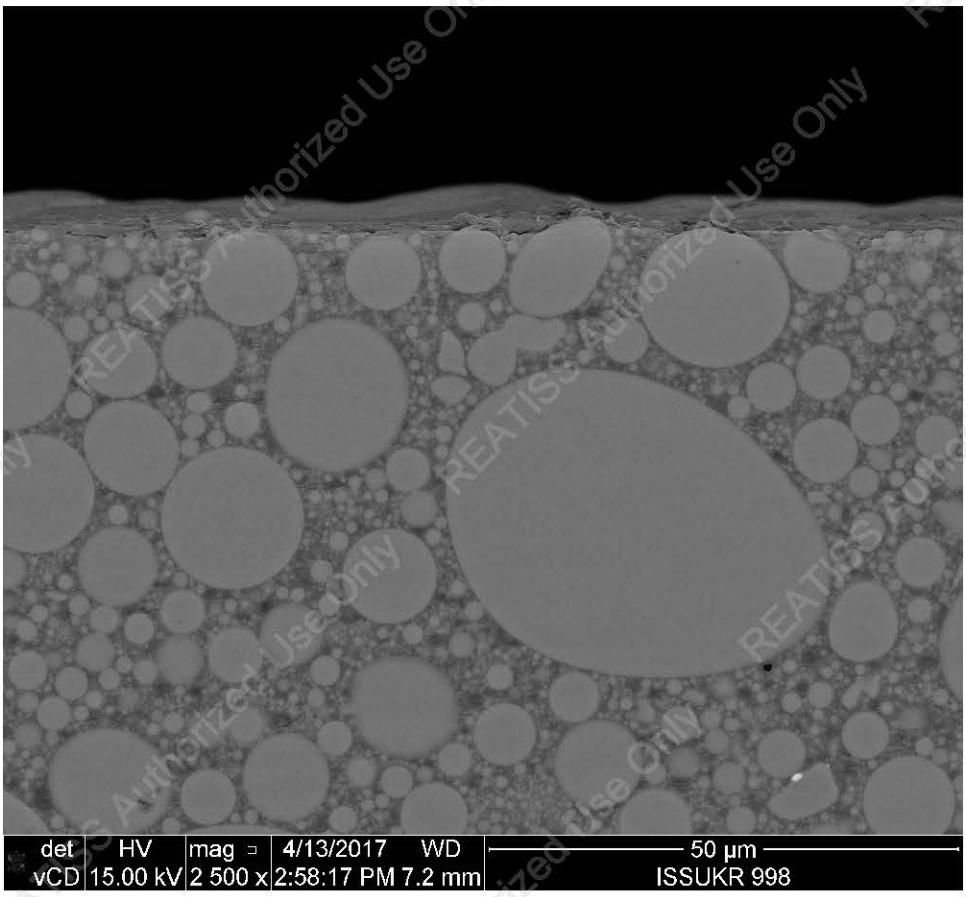

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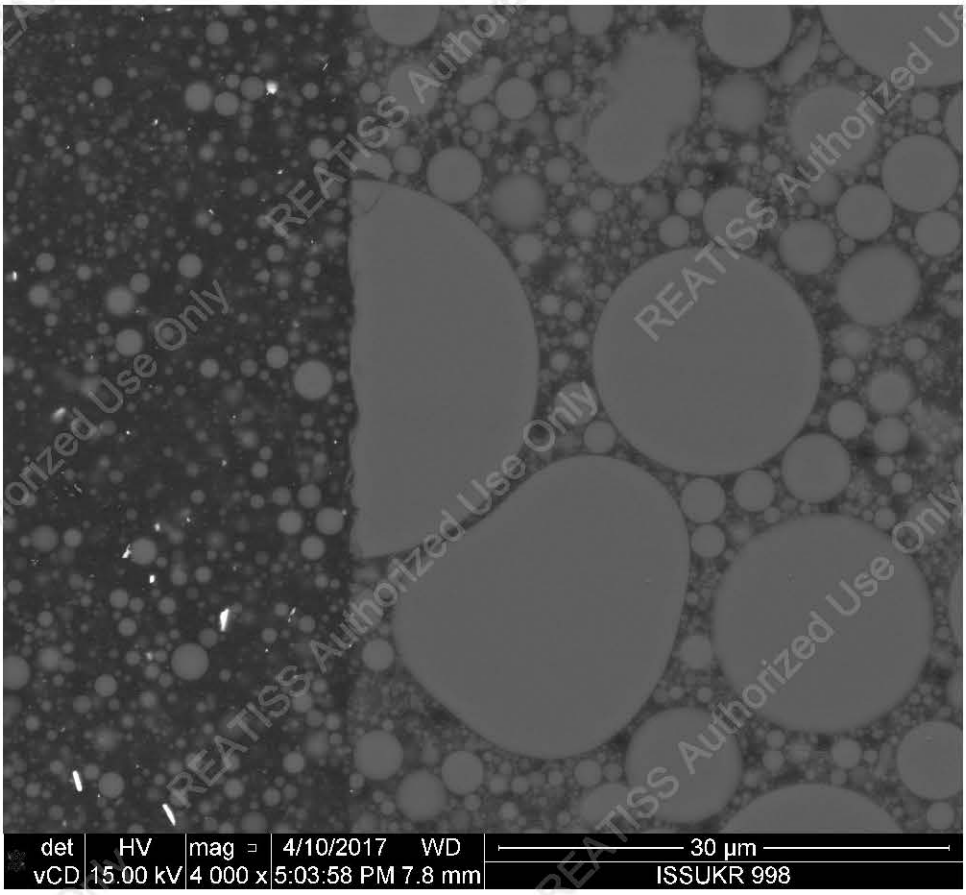


Figure 29. Memory package mold compound edge

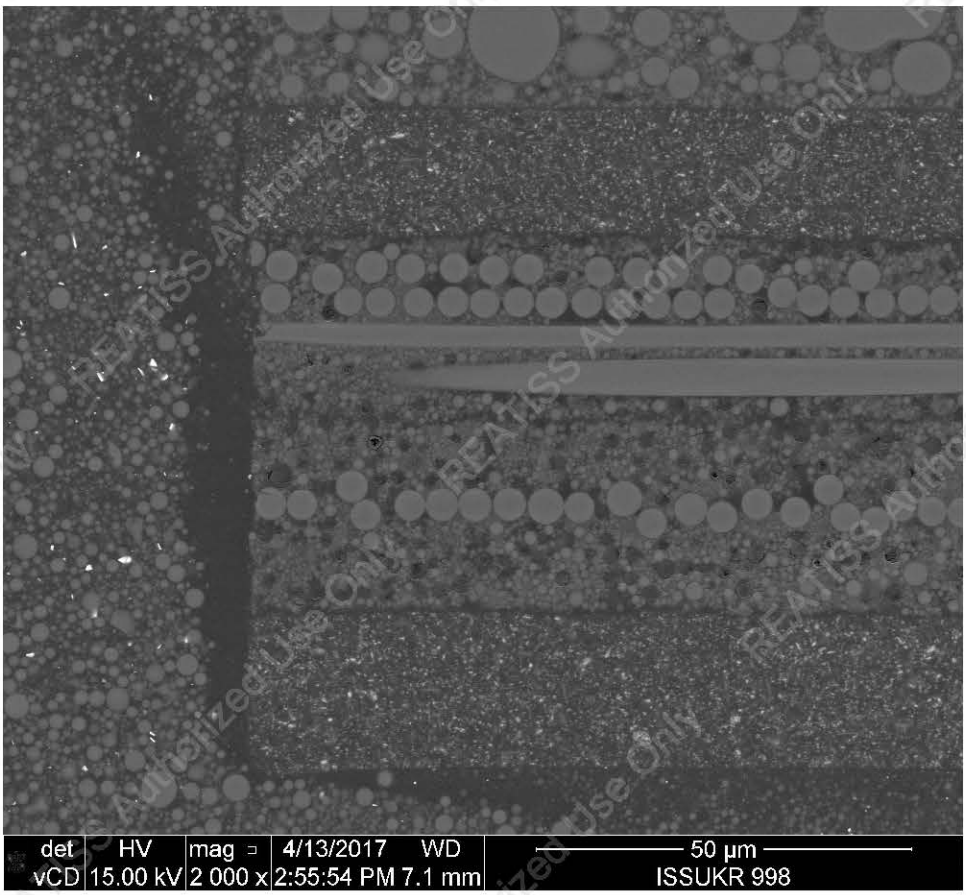
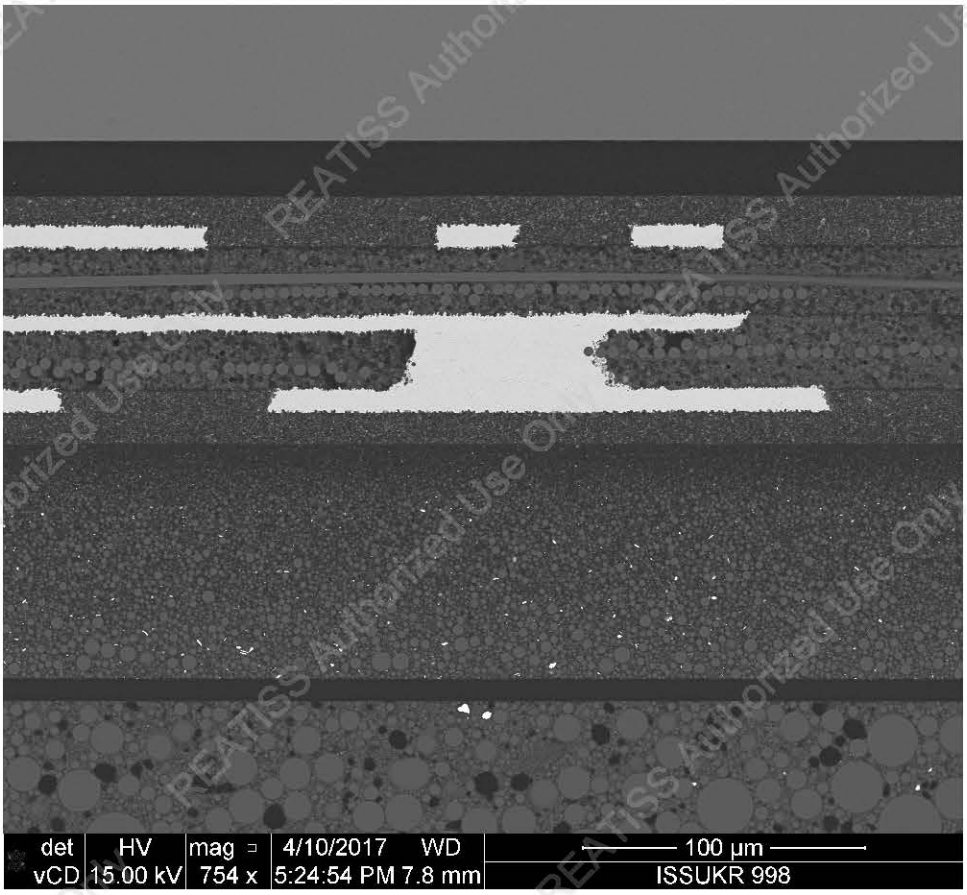


Figure 30. Memory package substrate edge



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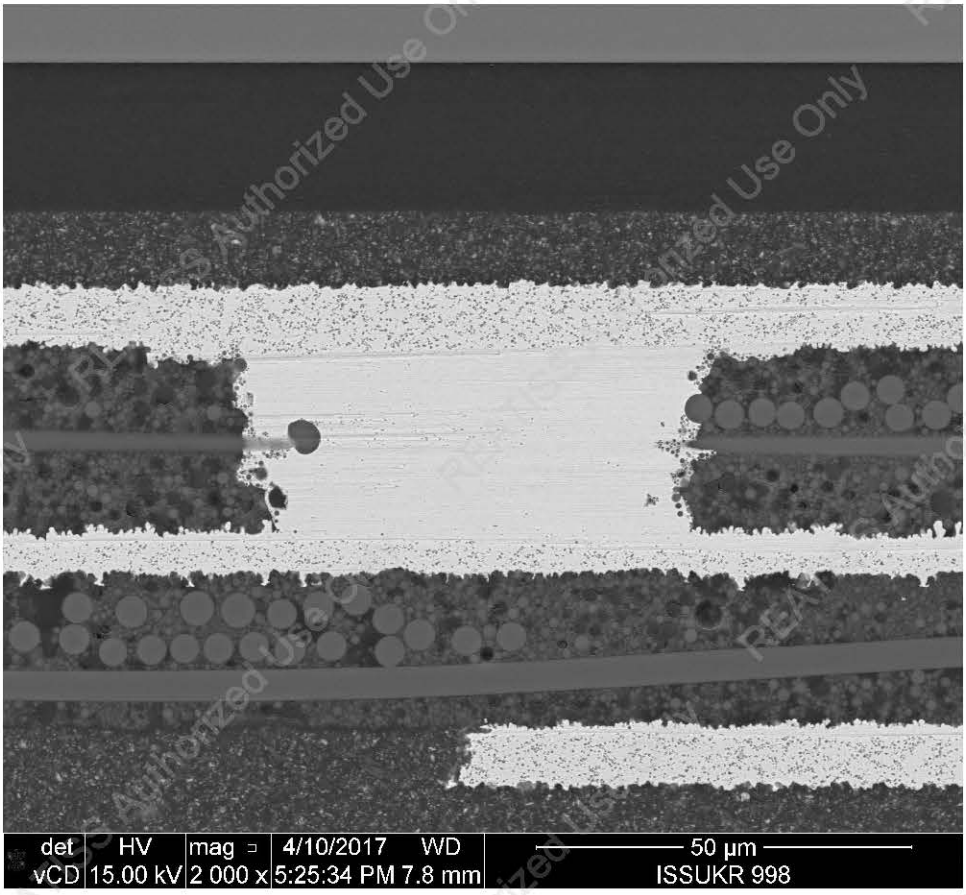

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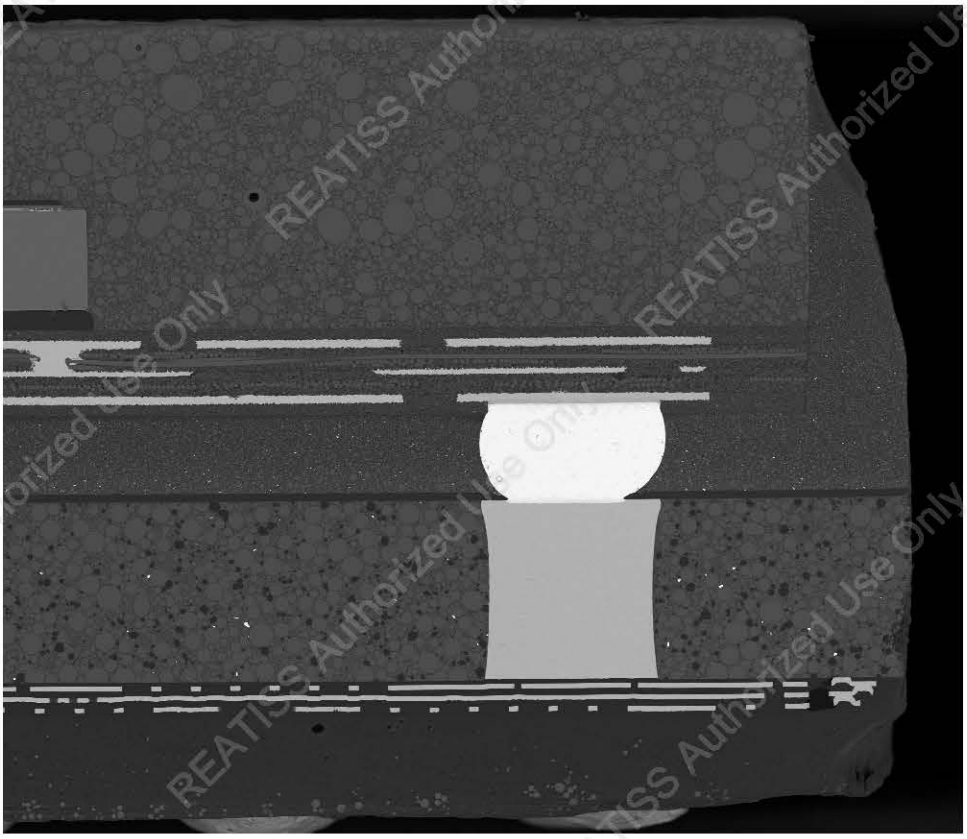

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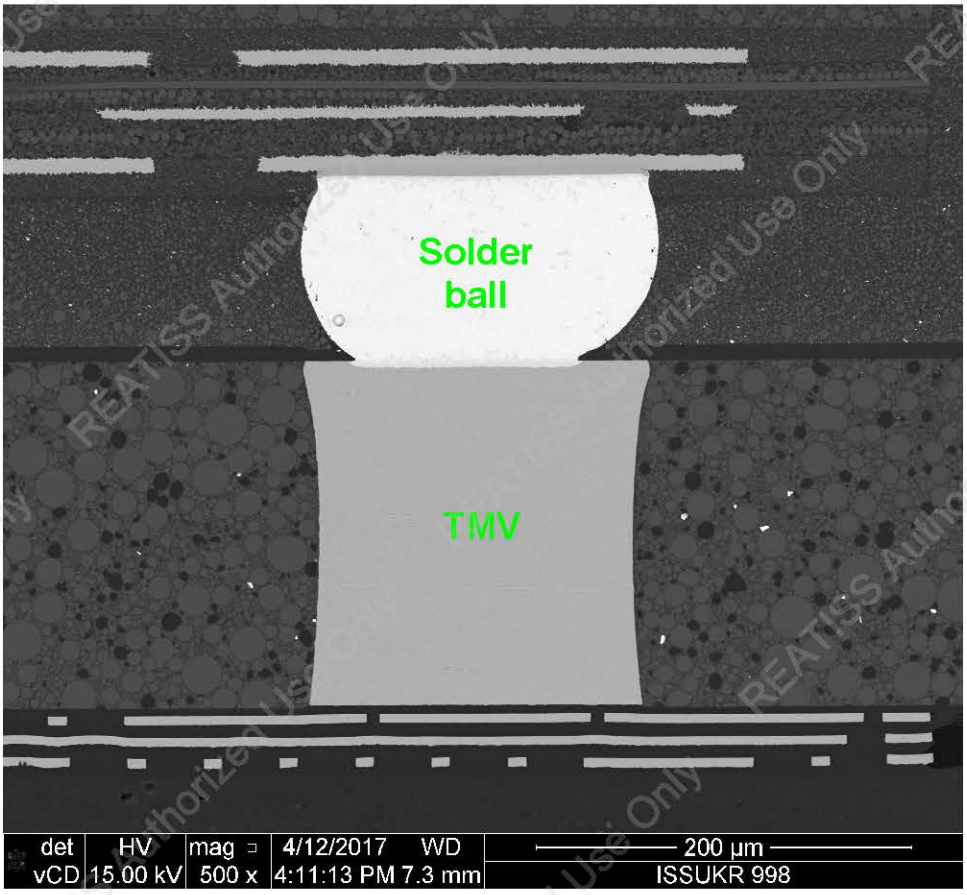

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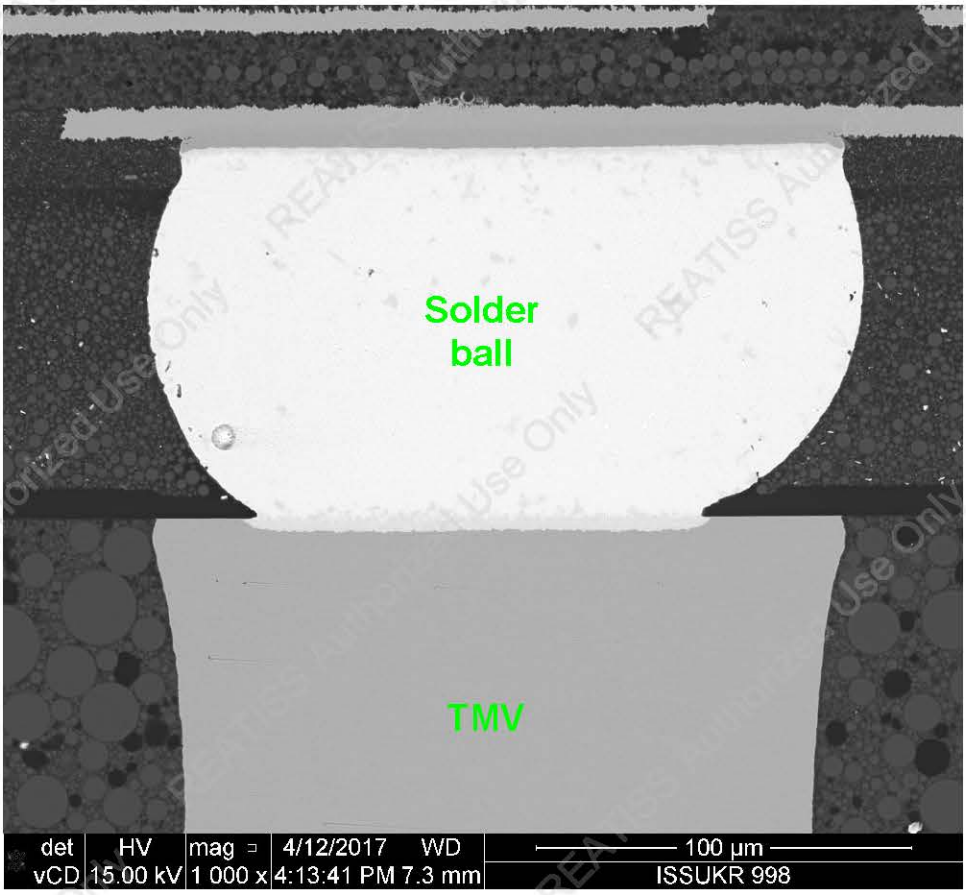


Figure 35. Memory package contact pad and package connection solder ball

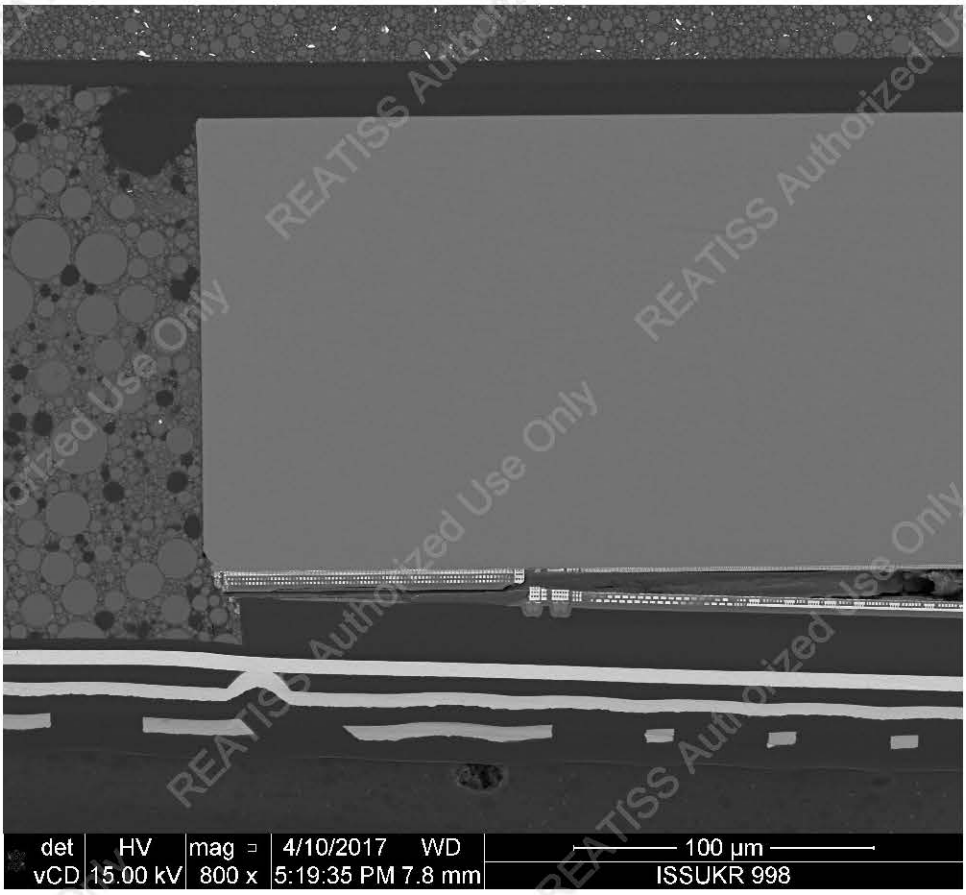


Figure 36. Processor die assembly

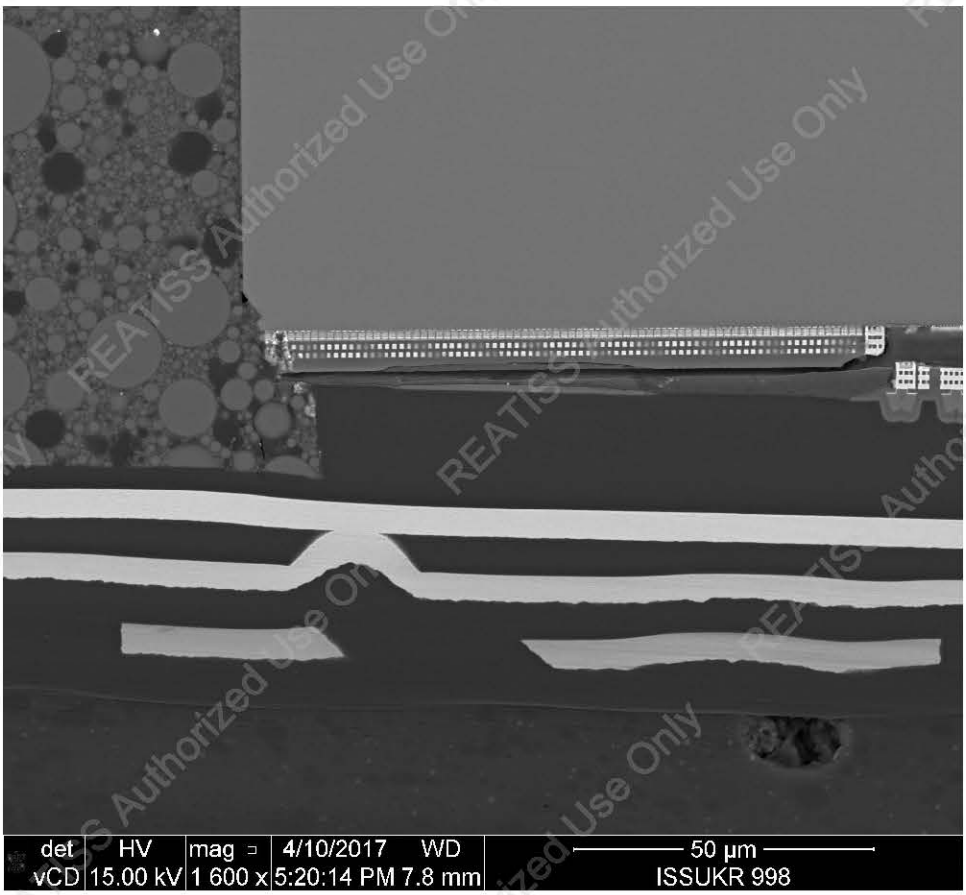
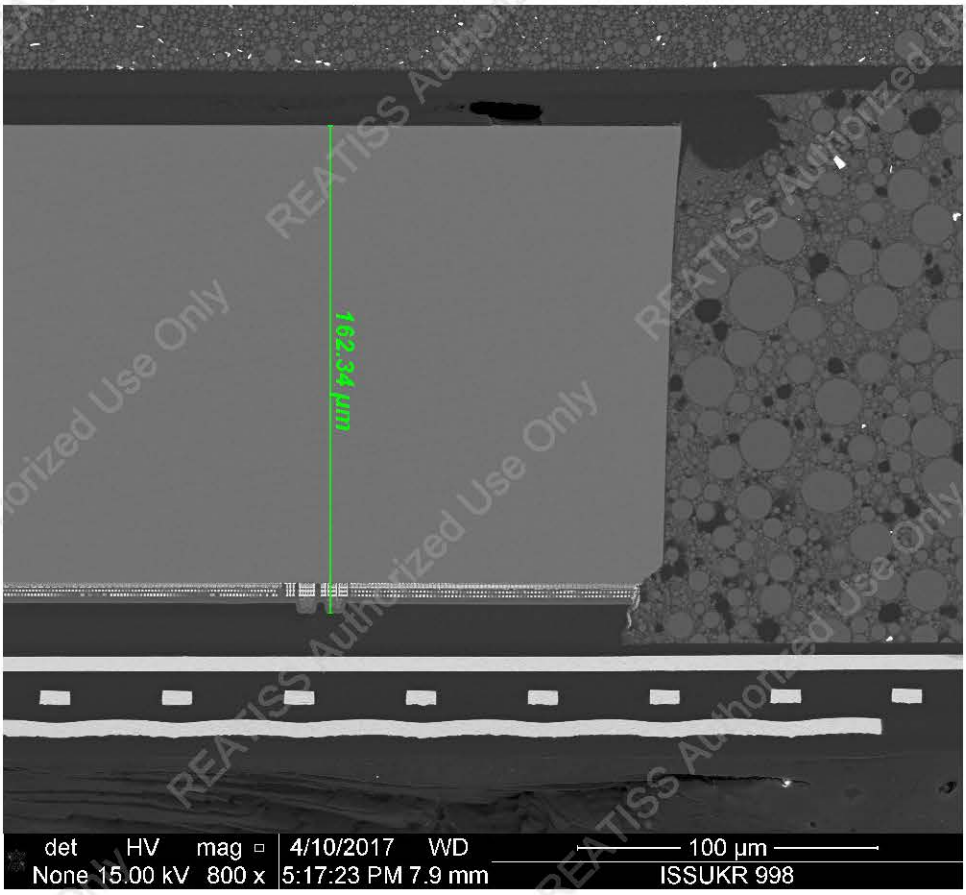


Figure 37. Processor die corner and encapsulation



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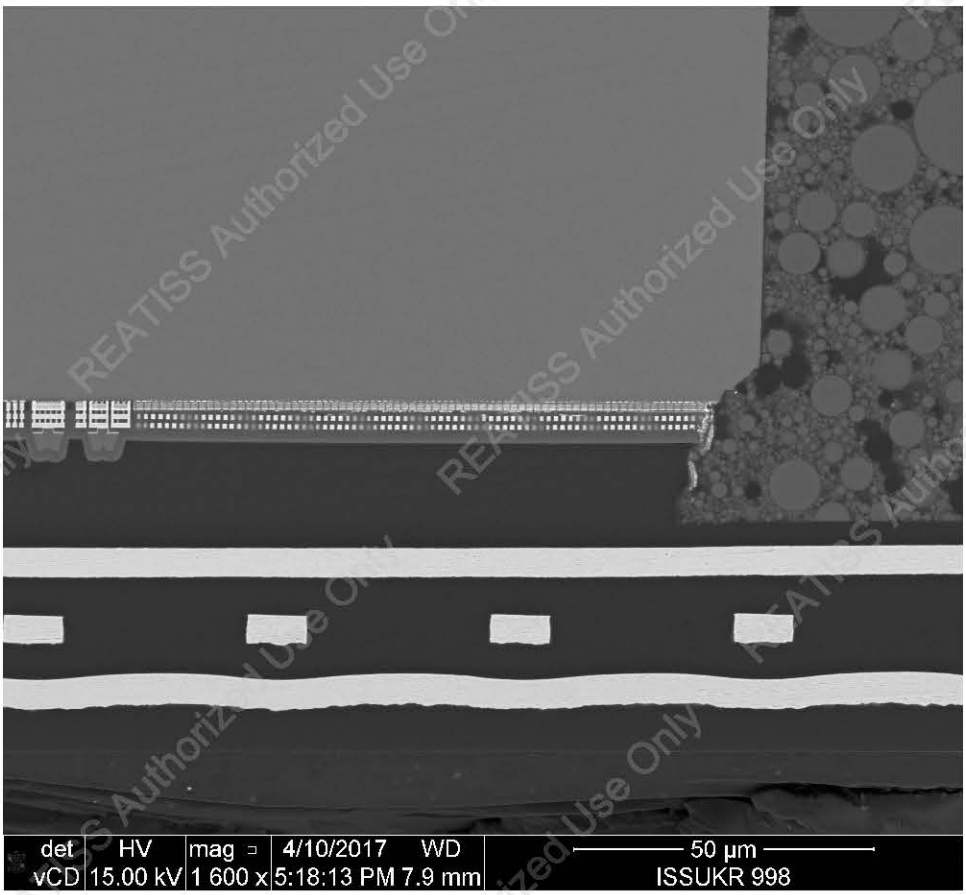
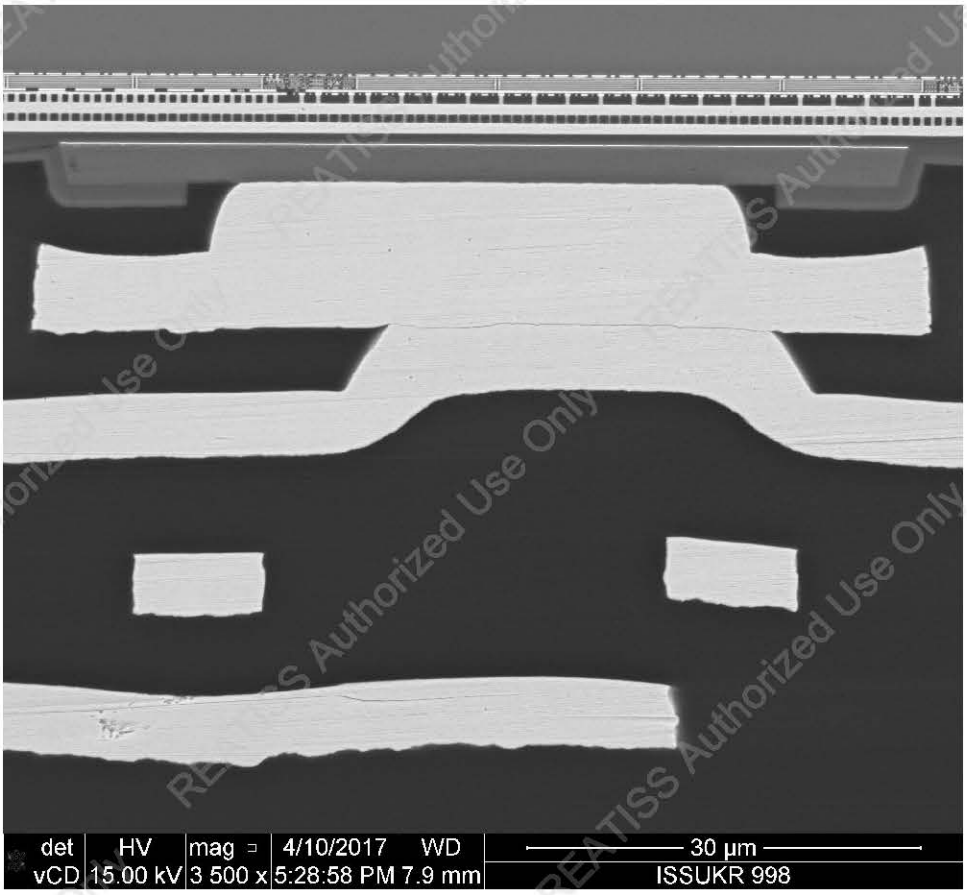


Figure 39. Processor die corner and encapsulation



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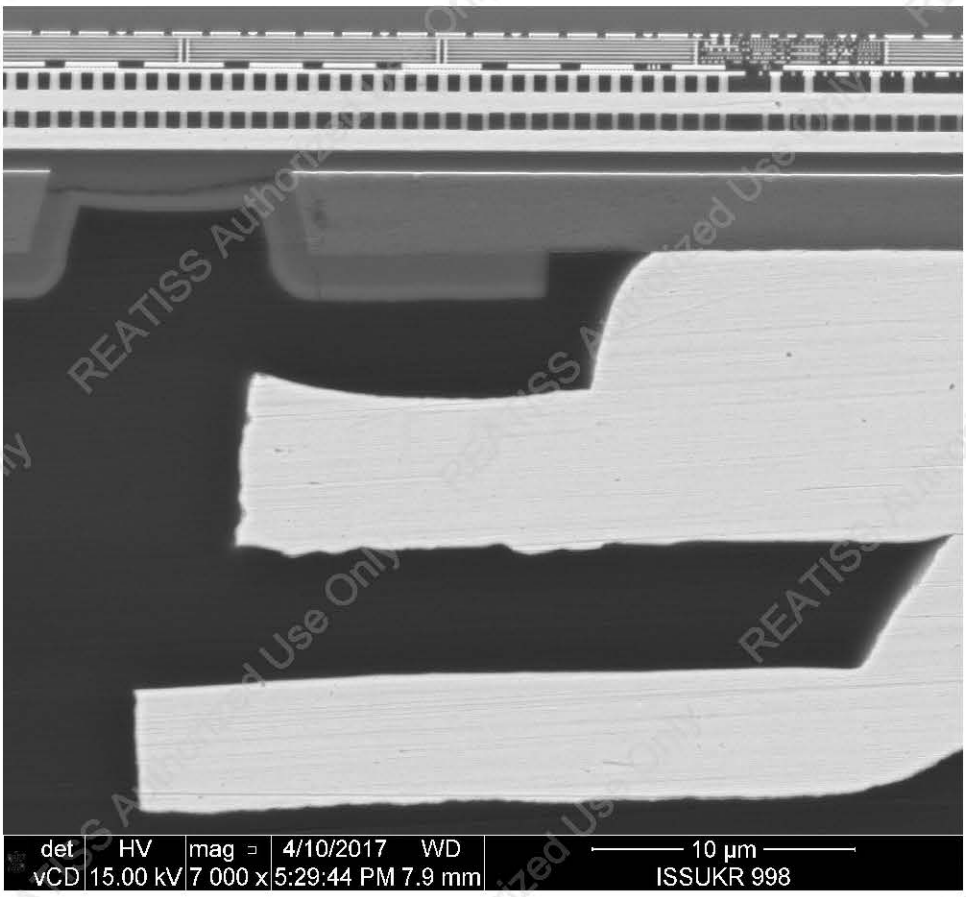

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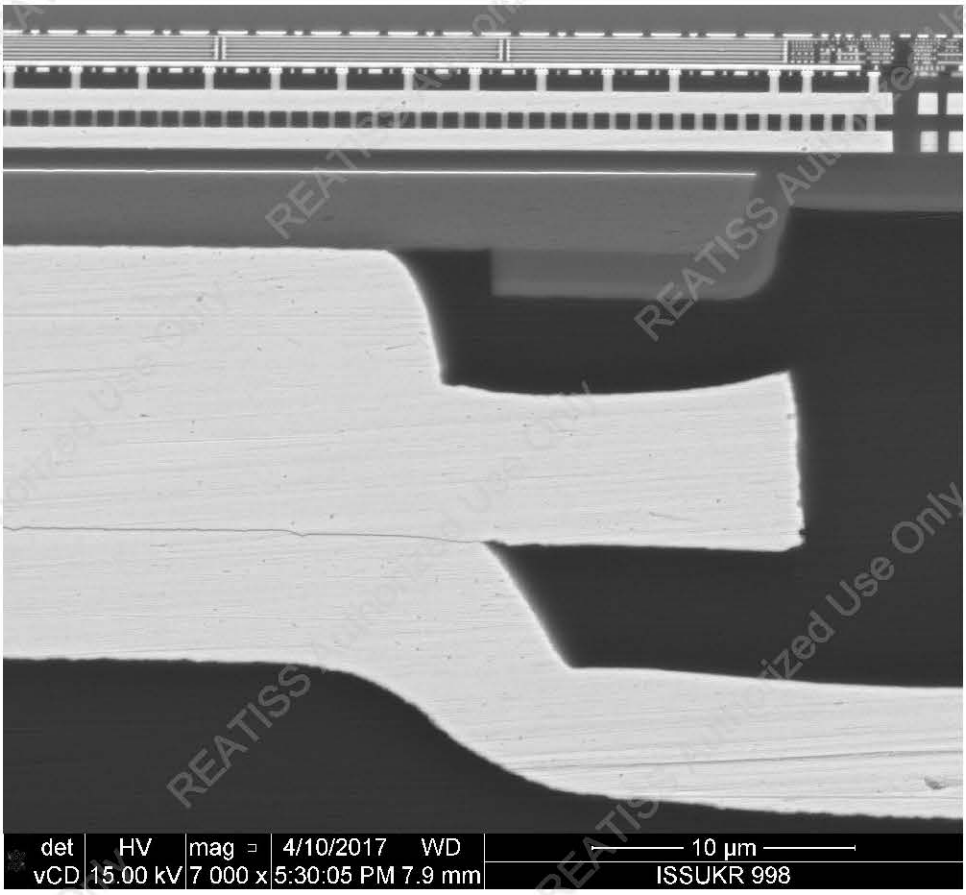

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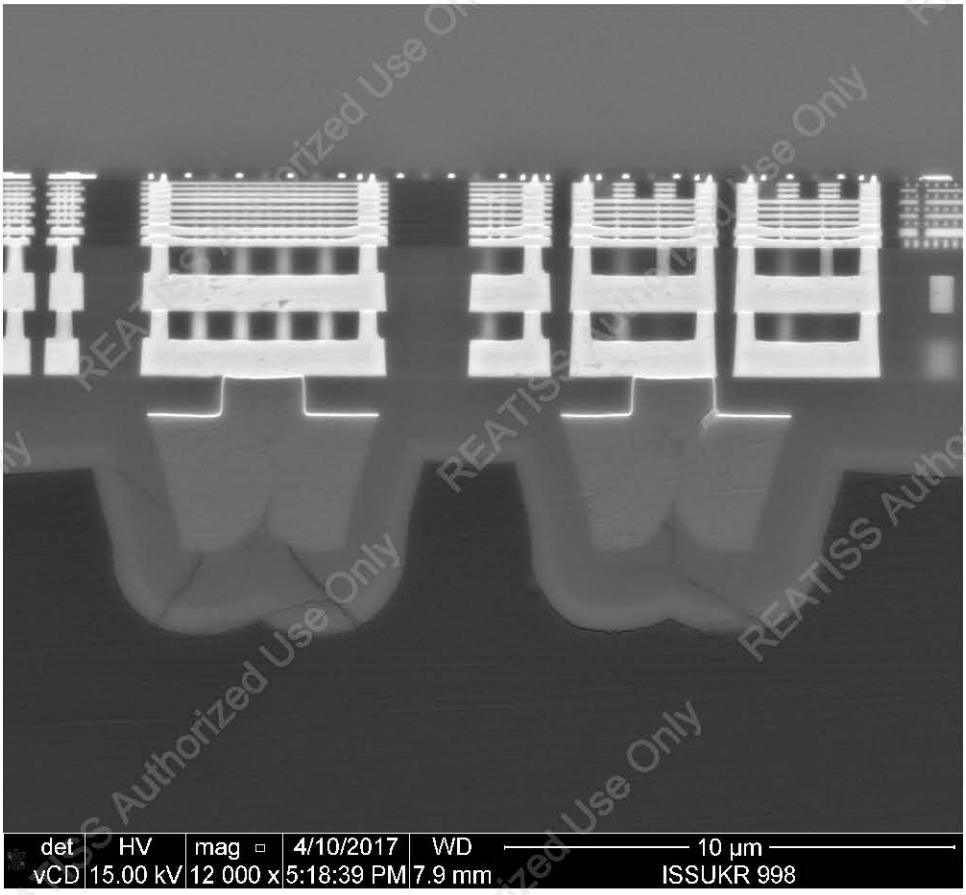

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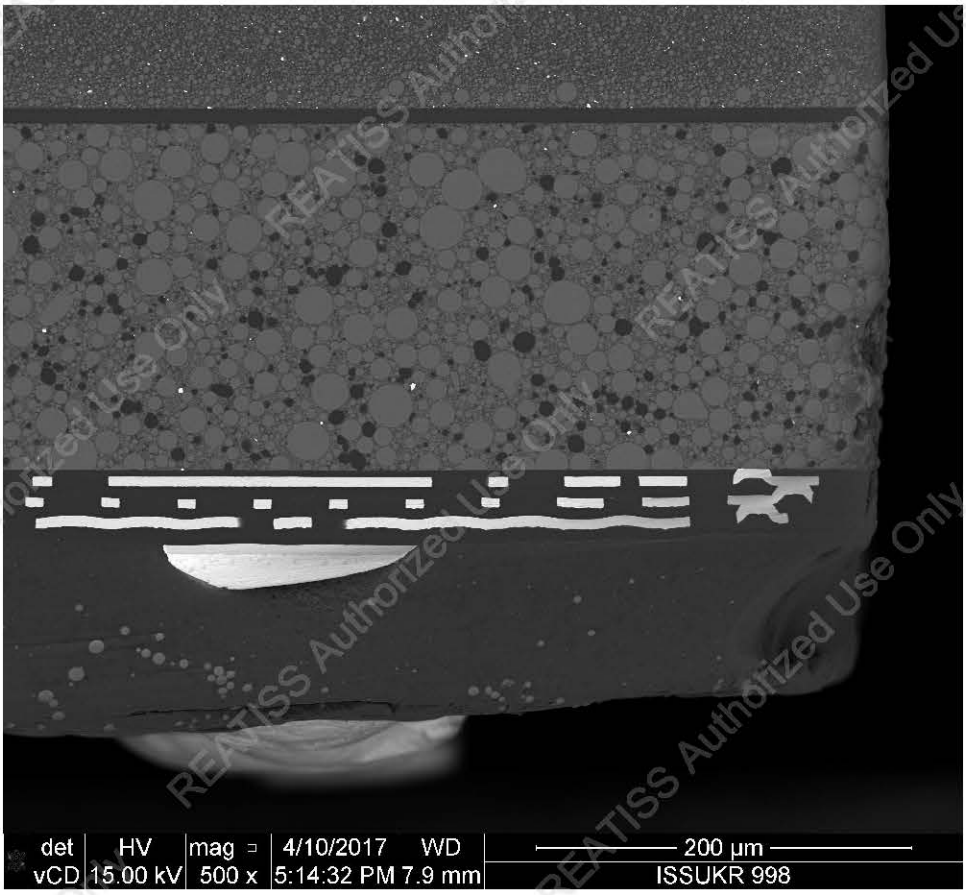


Figure 44. Processor package edge

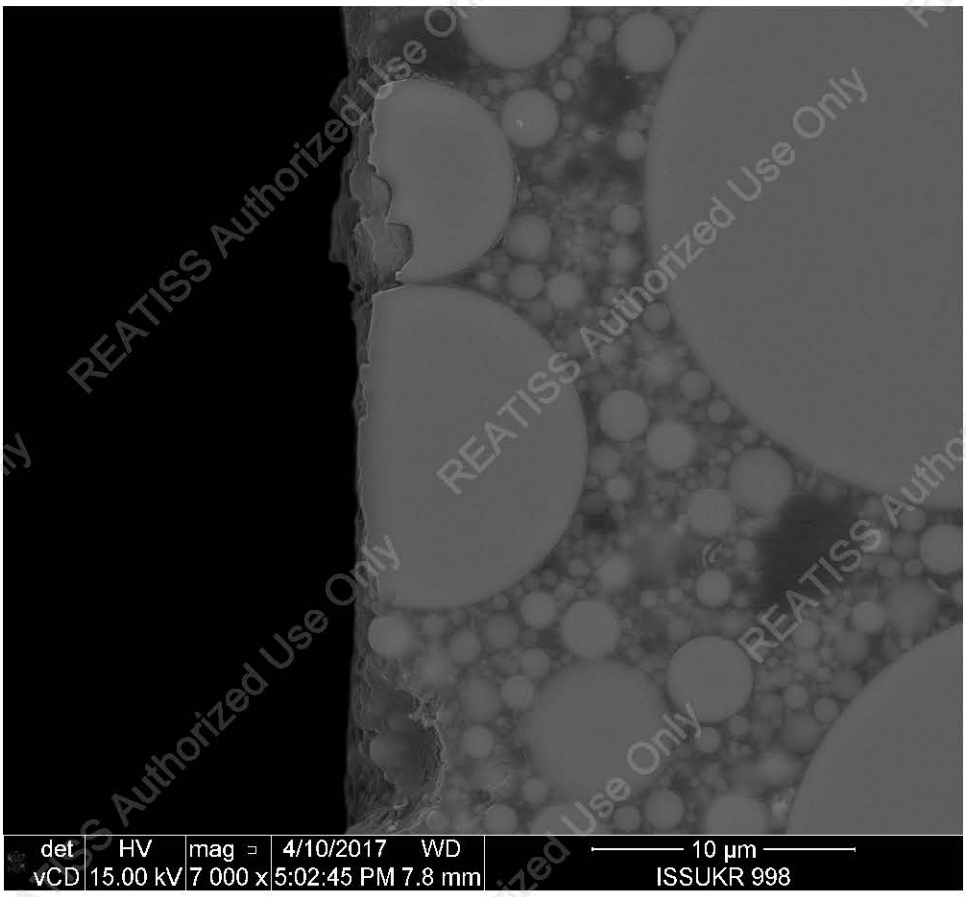


Figure 45. Processor package mold compound edge

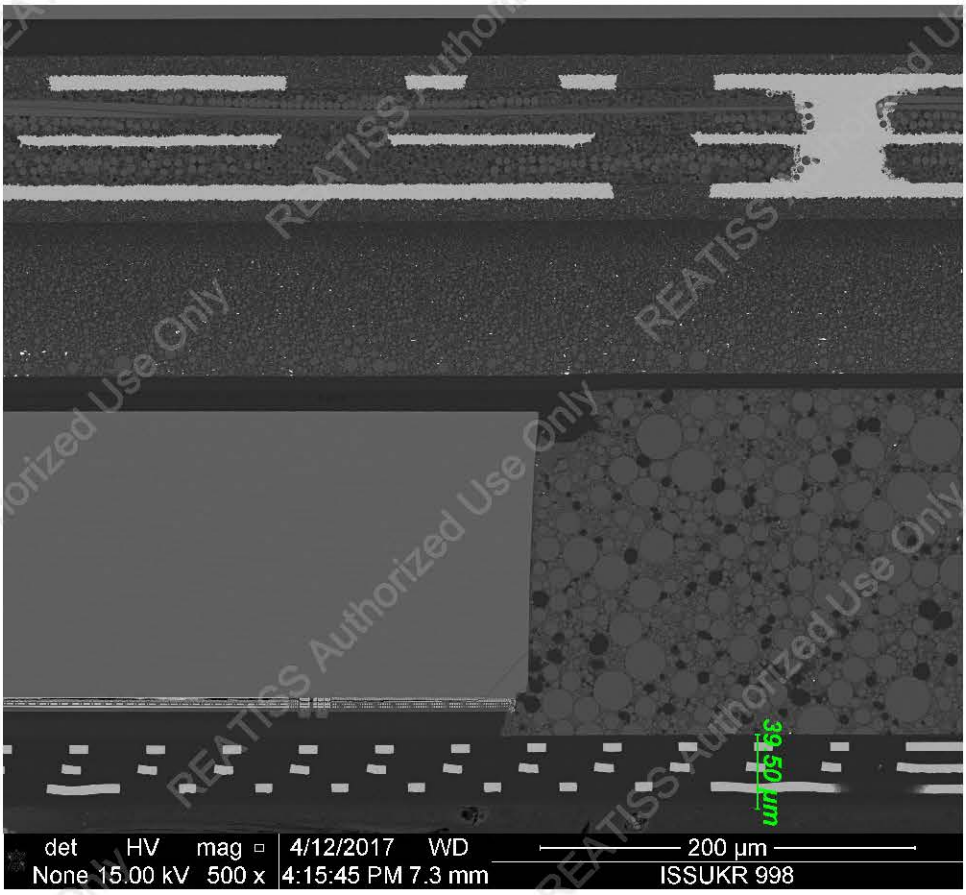


Figure 46. Processor package substrate and die

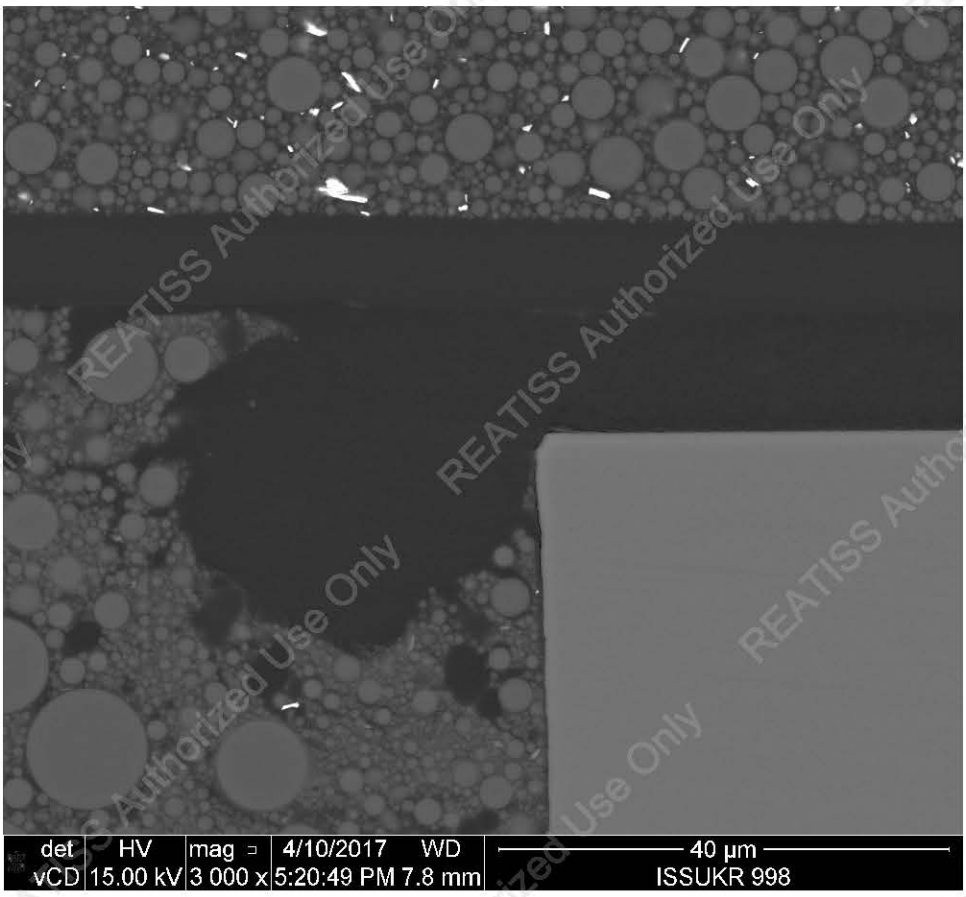


Figure 47. Processor die corner

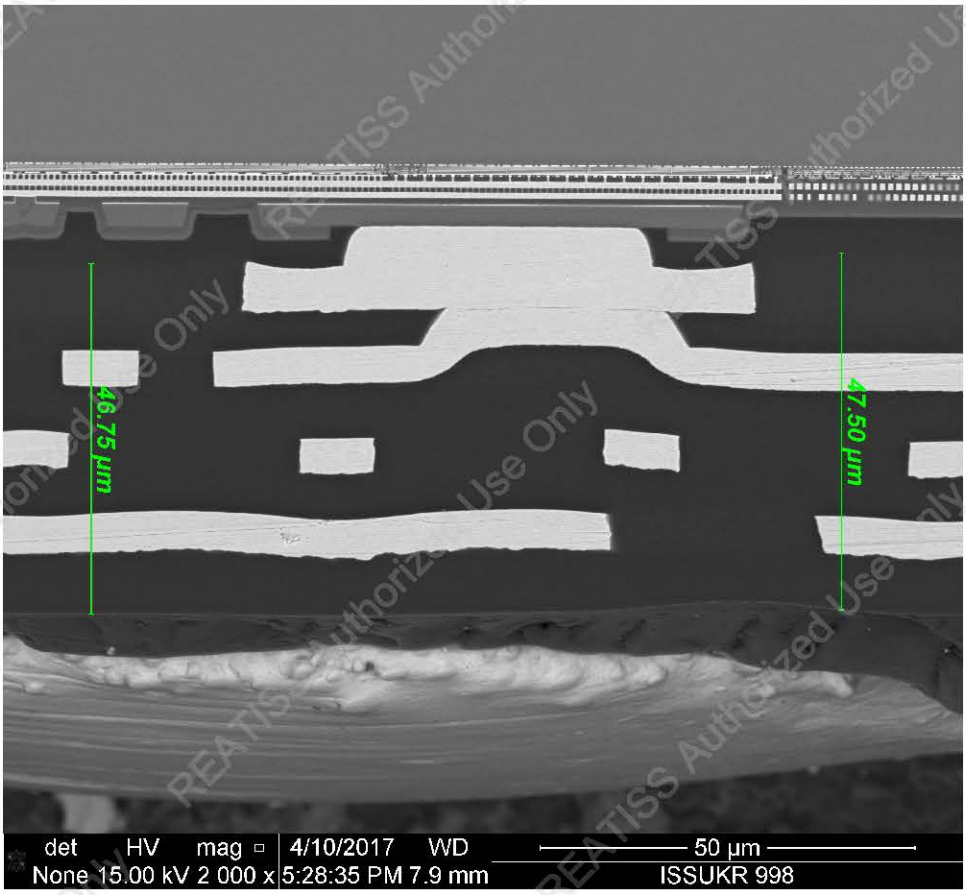
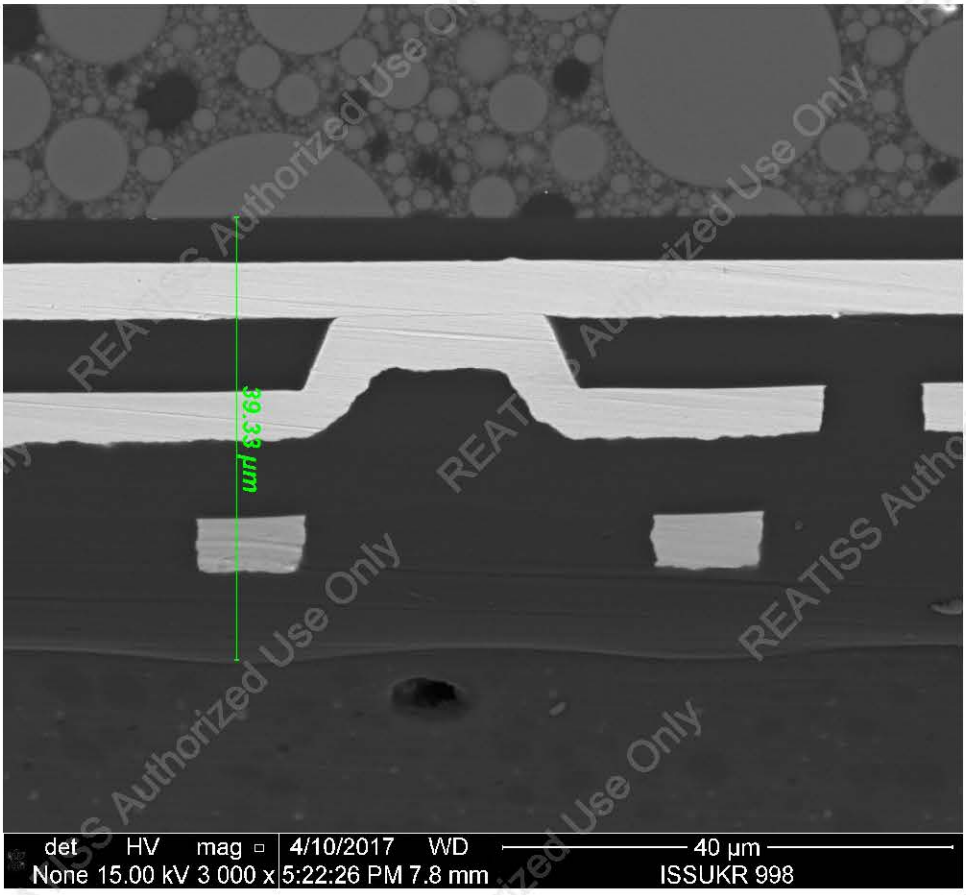


Figure 48. Processor package substrate



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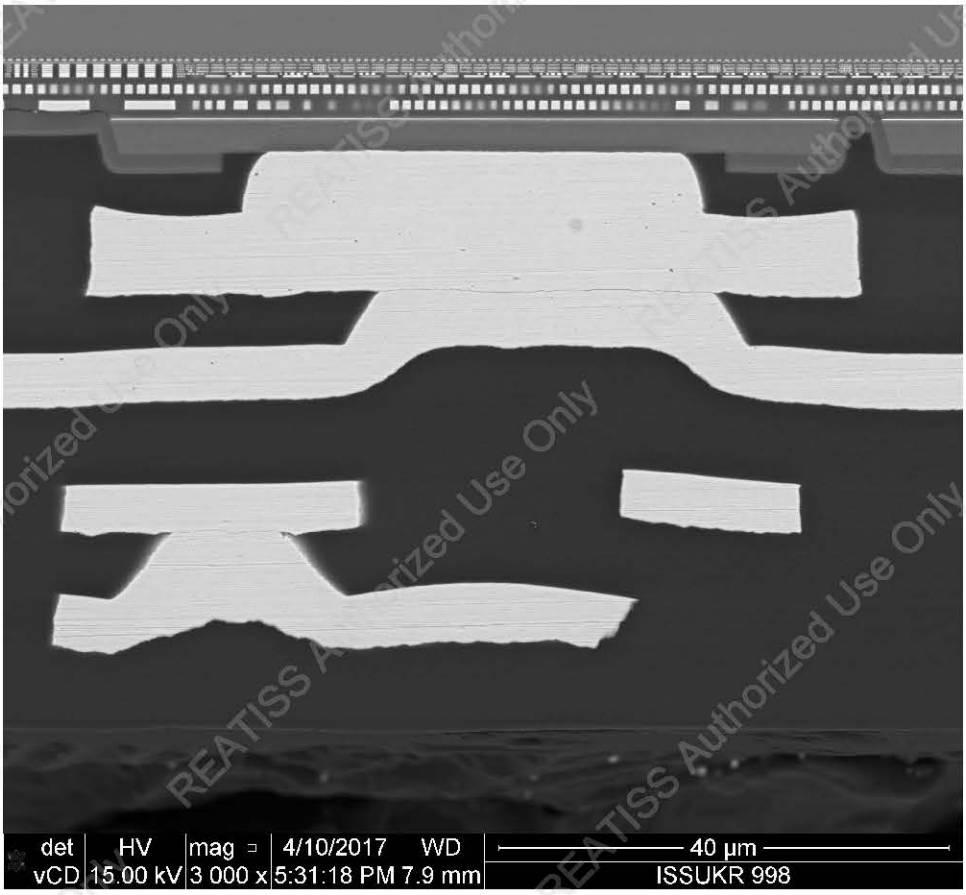

Figure 50. Processor bond pad and package substrate via

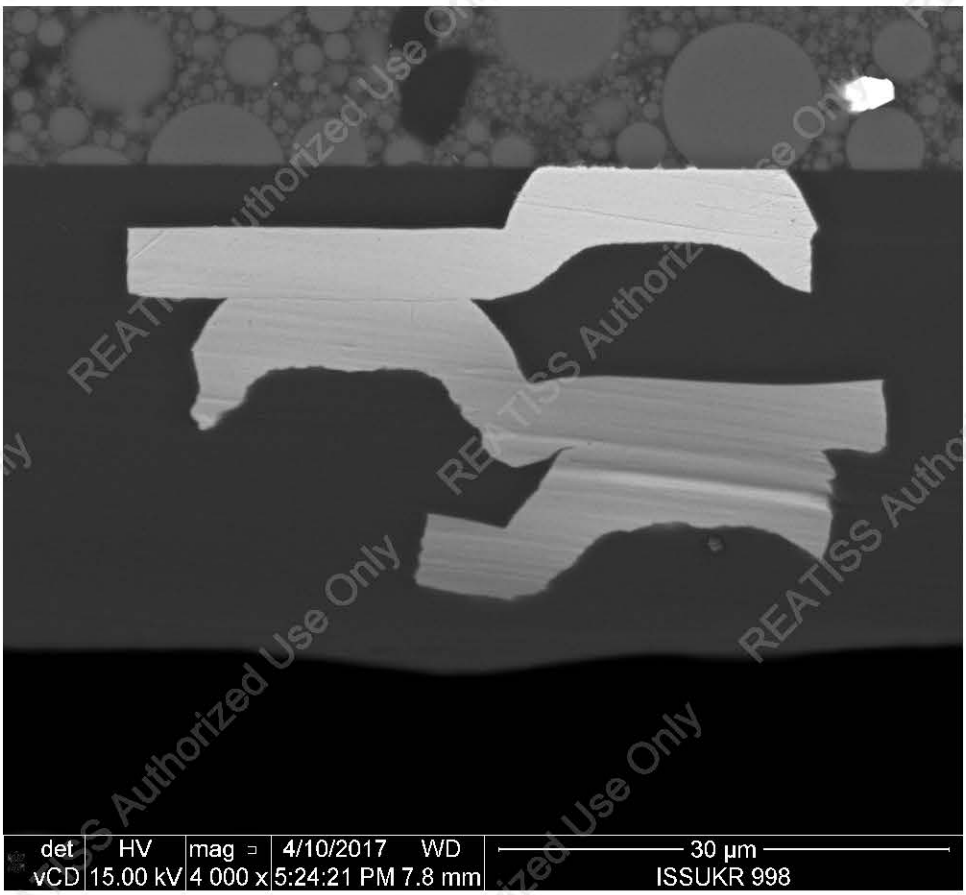

Figure 51. Processor package vias

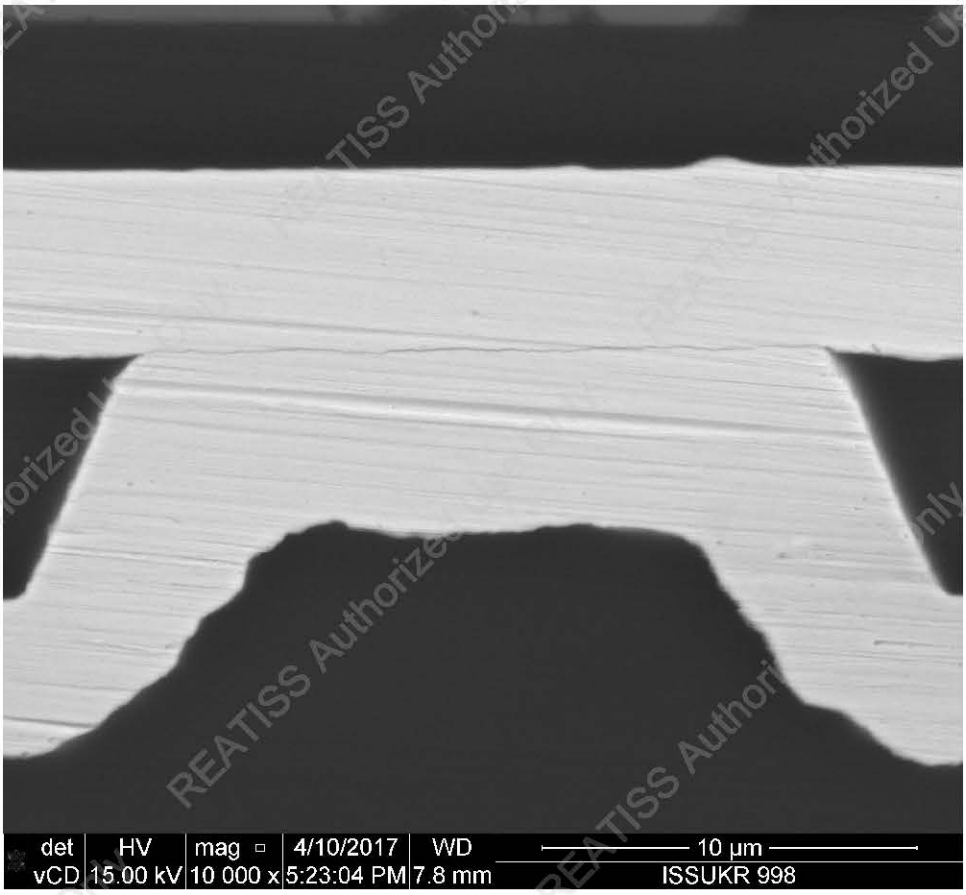

Figure 52. Processor package substrate via

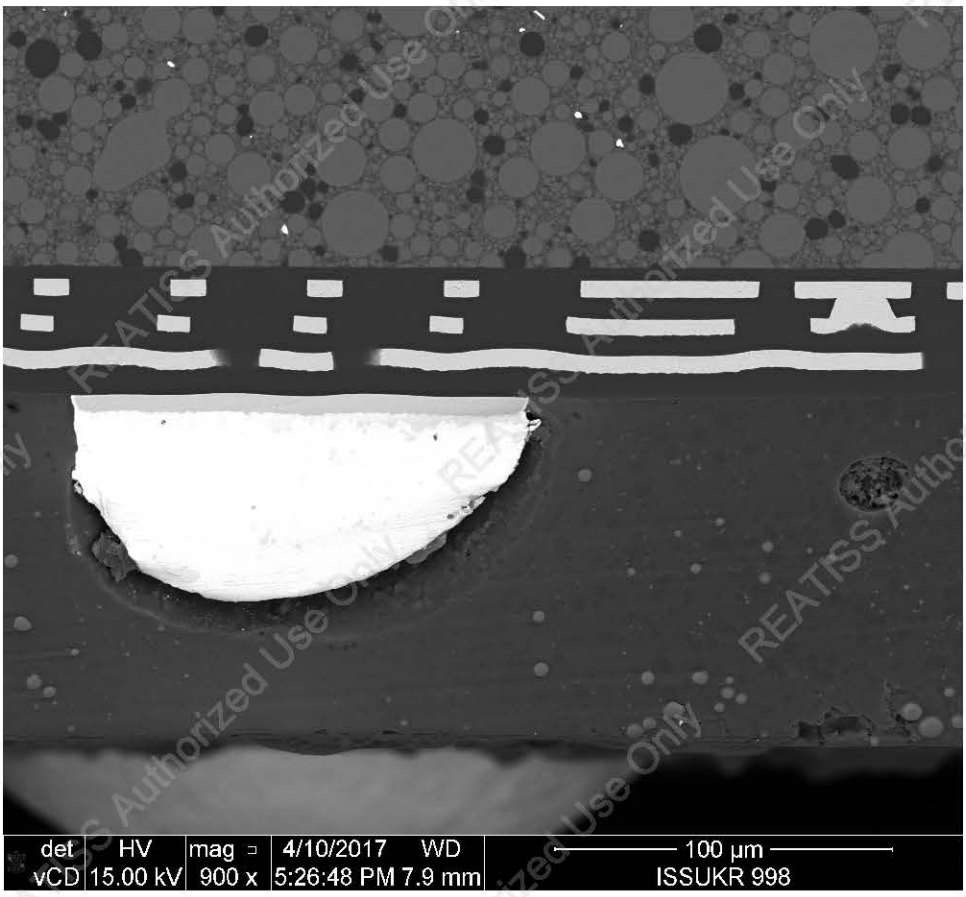

Figure 53. Processor contact pad and ball

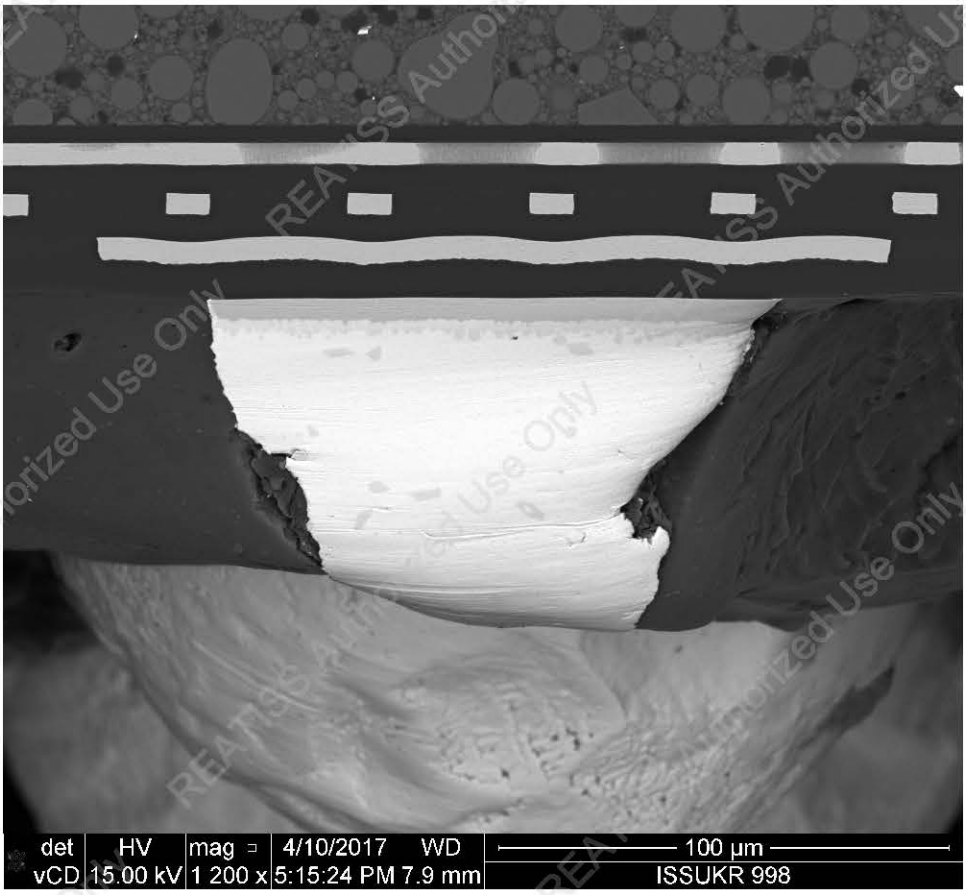

Figure 54. Processor contact pad and ball

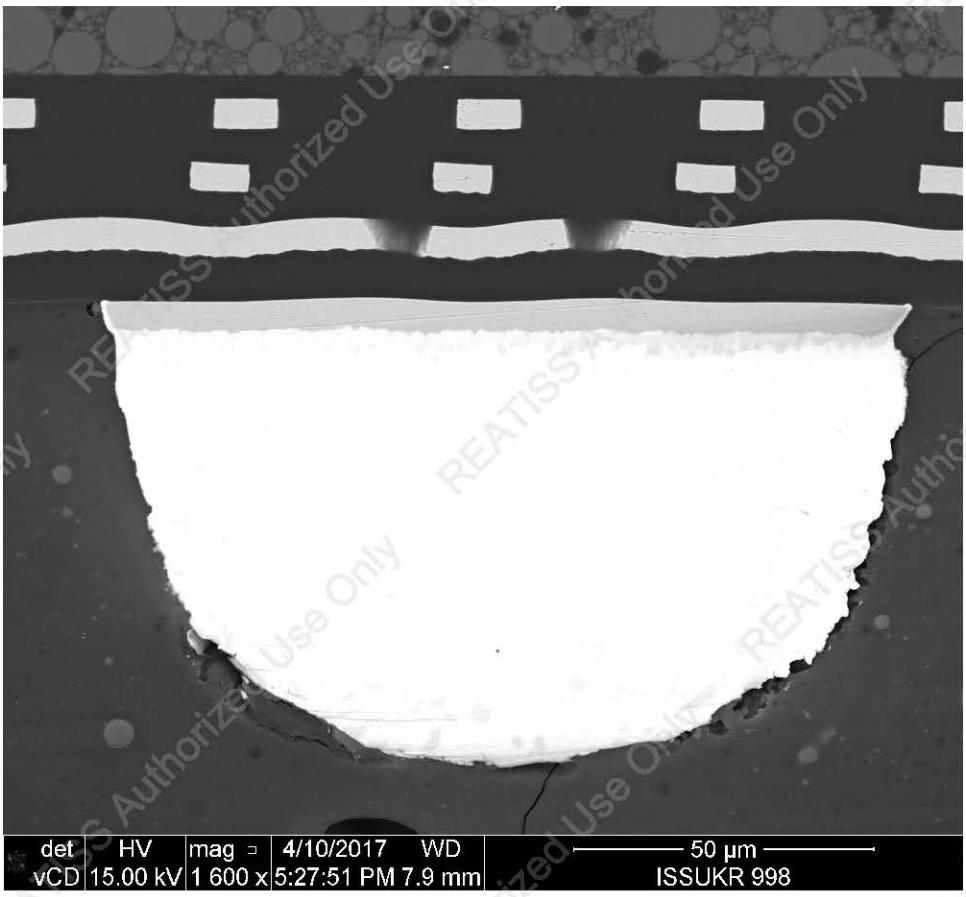

Figure 55. Processor contact pad and ball

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Figure 56. Processor die bond pad and via

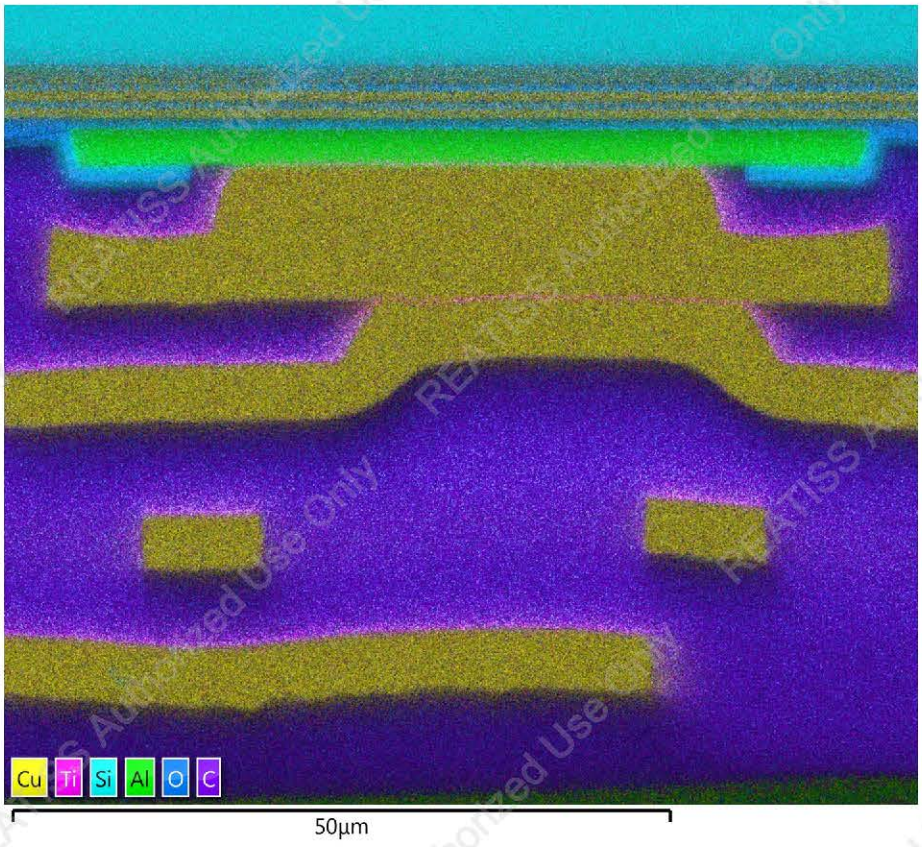


Figure 57. Layered EDX map of processor die bond pad and via

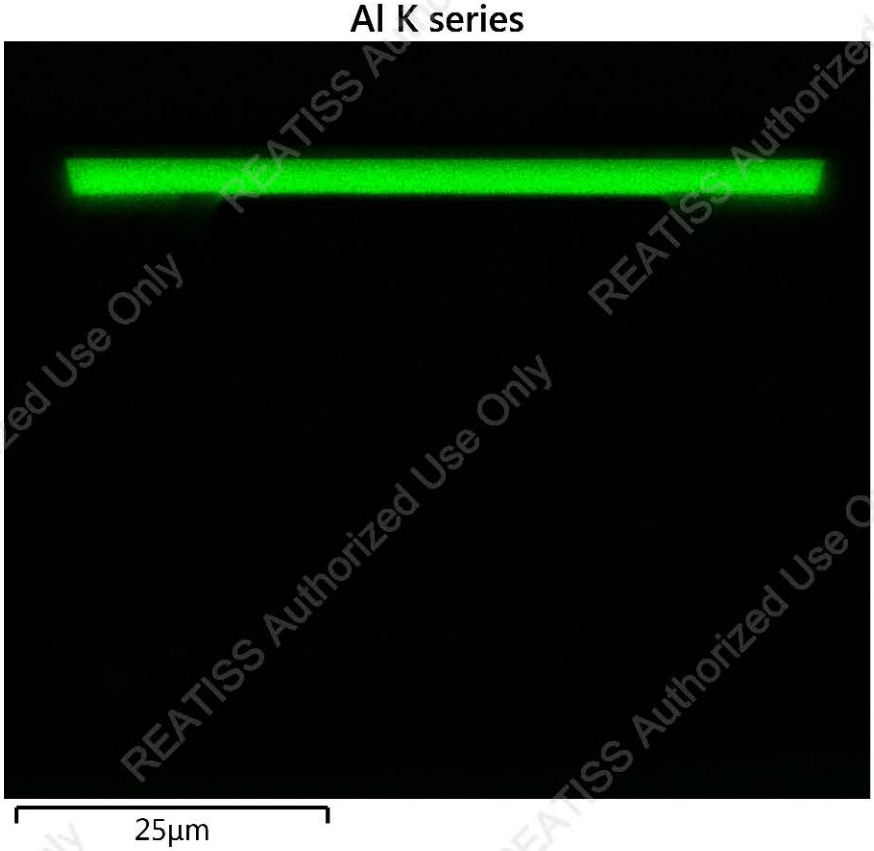
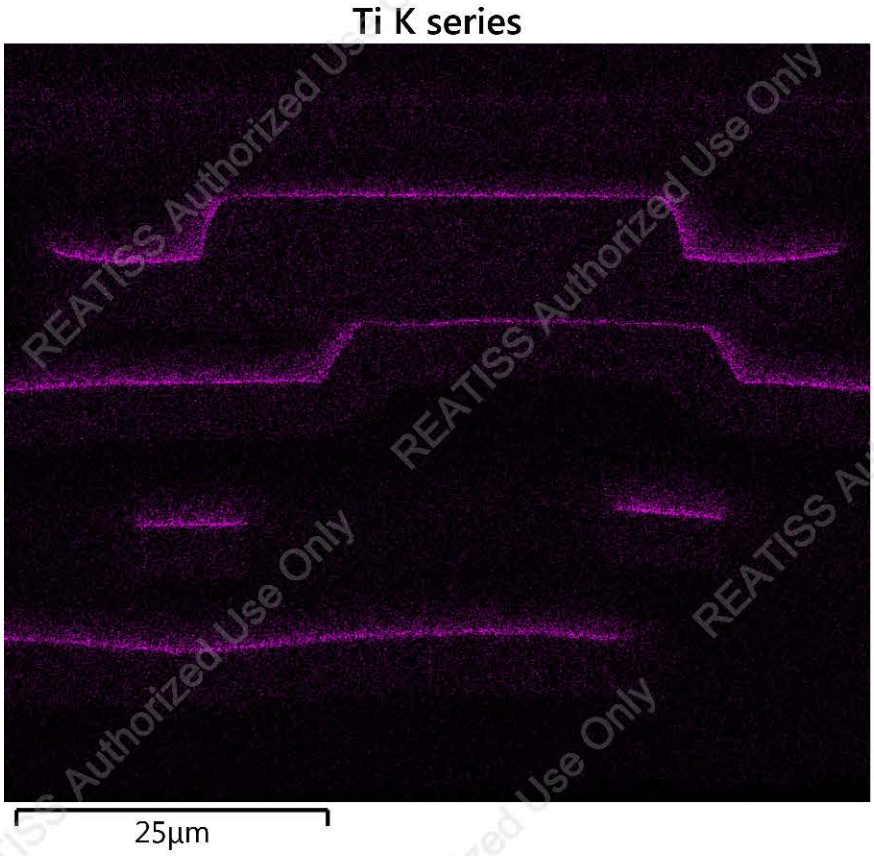


Figure 58. Aluminum EDX map layer



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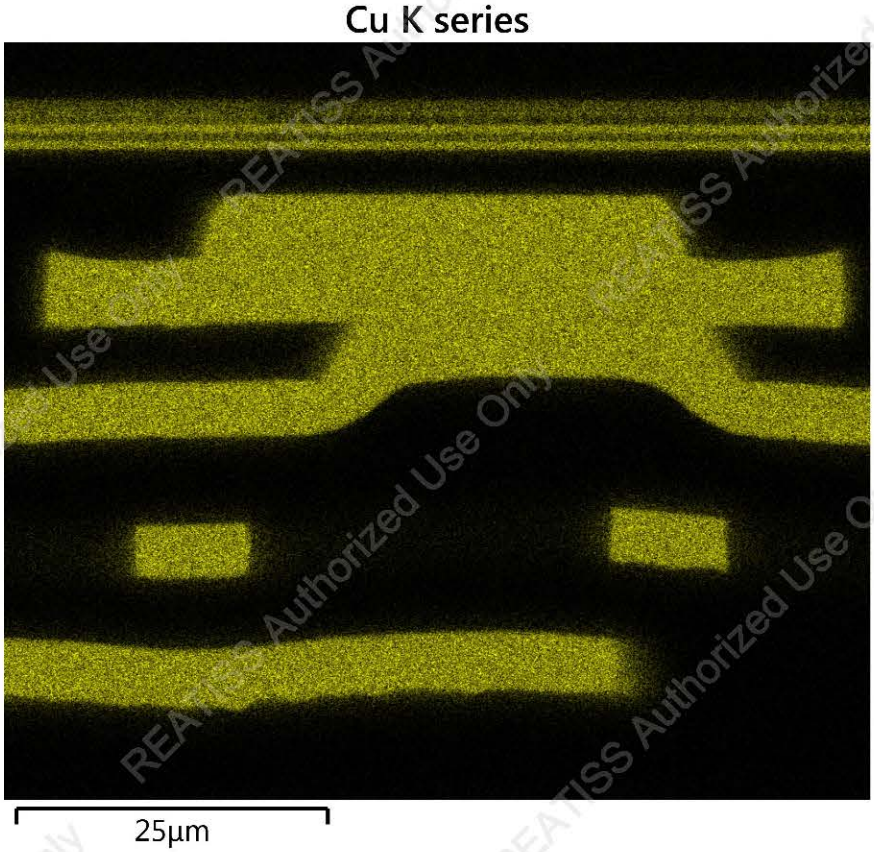

Figure 60. Copper EDX map layer

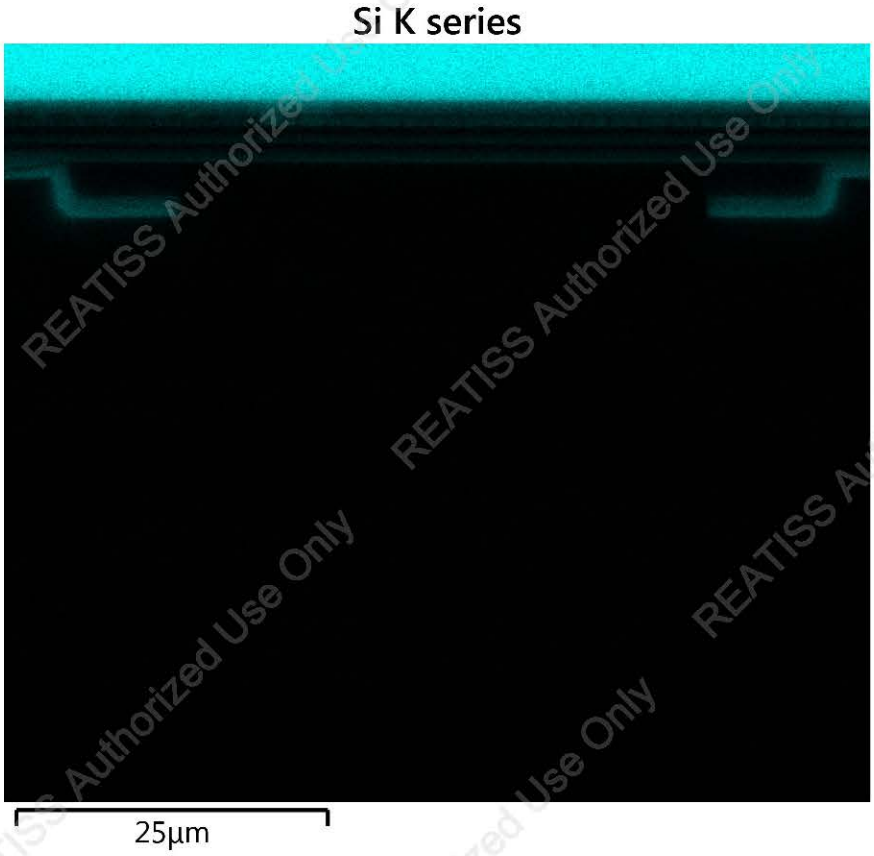

Figure 61. Silicon EDX map layer

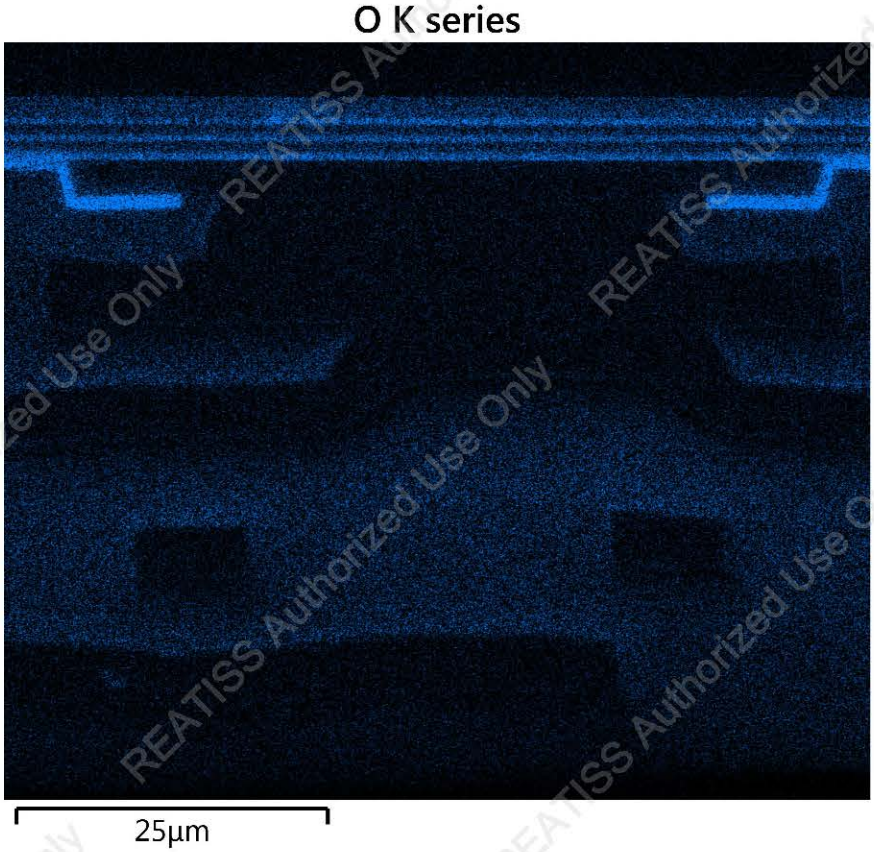

Figure 62. Oxygen EDX map layer

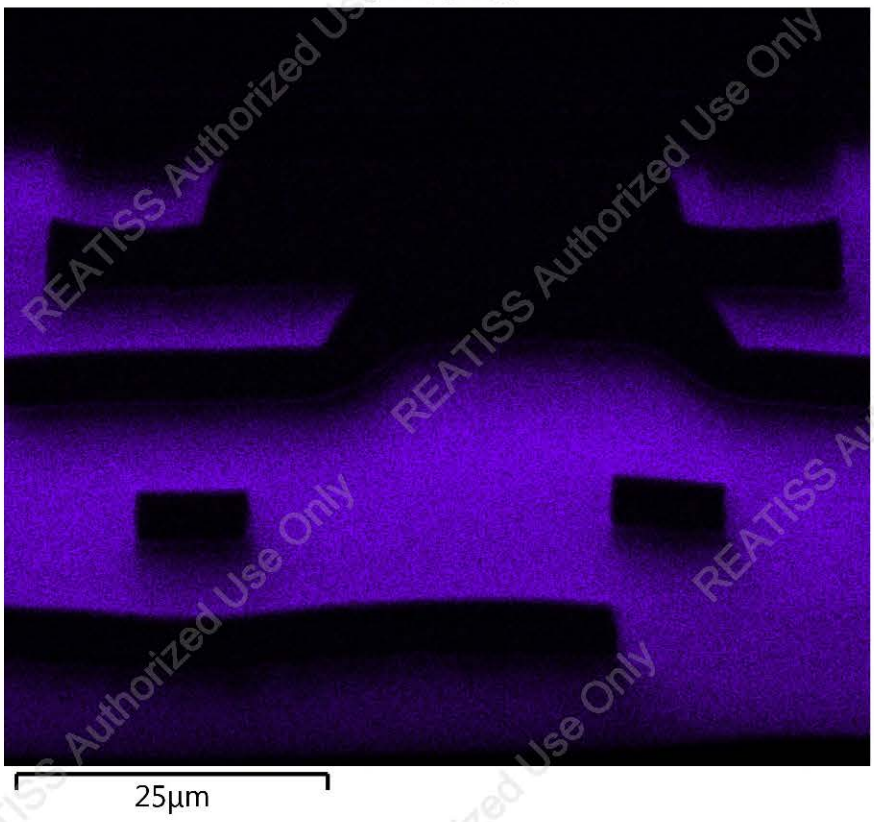

Figure 63. Carbon EDX map layer

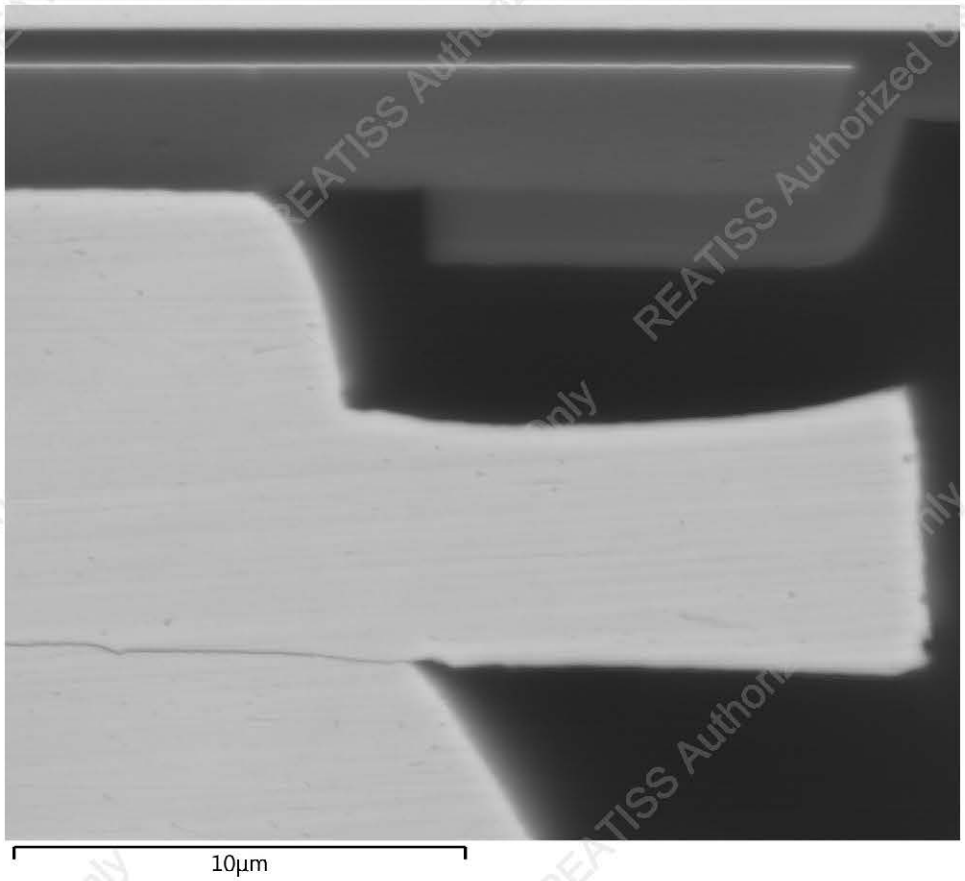

Figure 64. Processor die bond pad edge

Figure 65. Layered EDX map of processor die bond pad edge

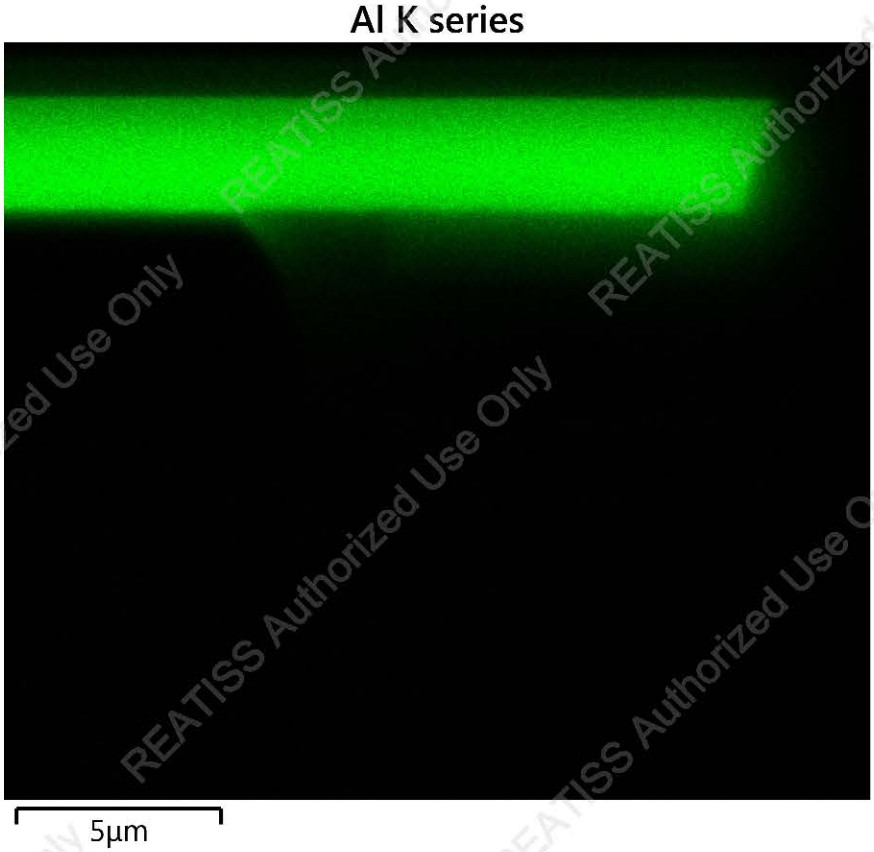

Figure 66. Aluminum EDX map layer

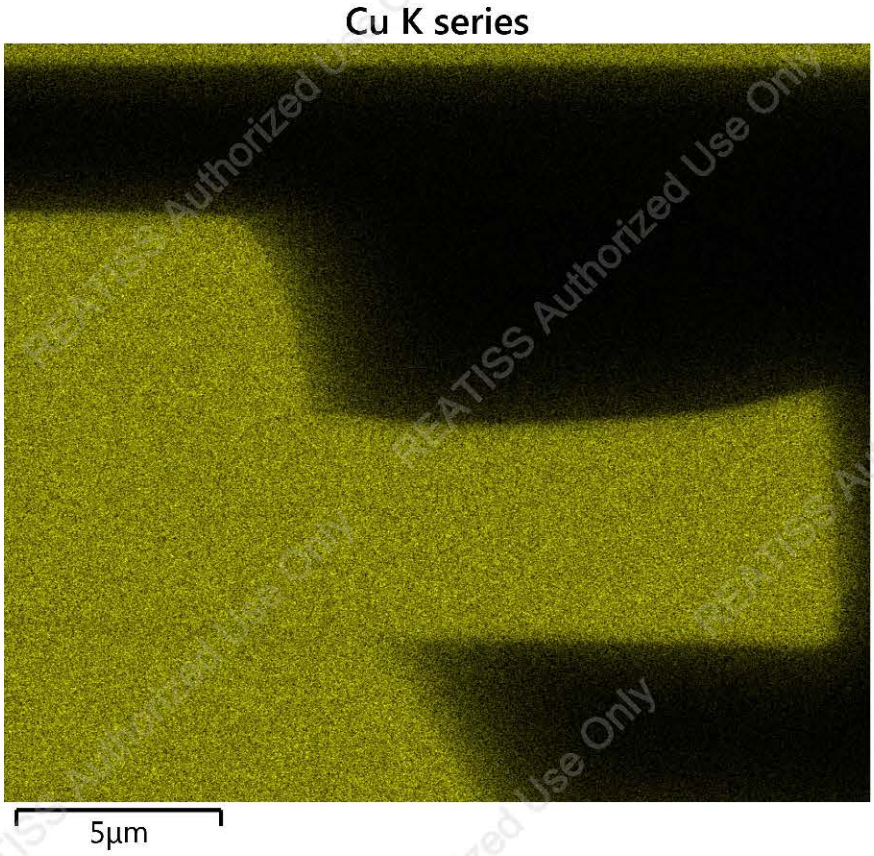

Figure 67. Copper EDX map layer

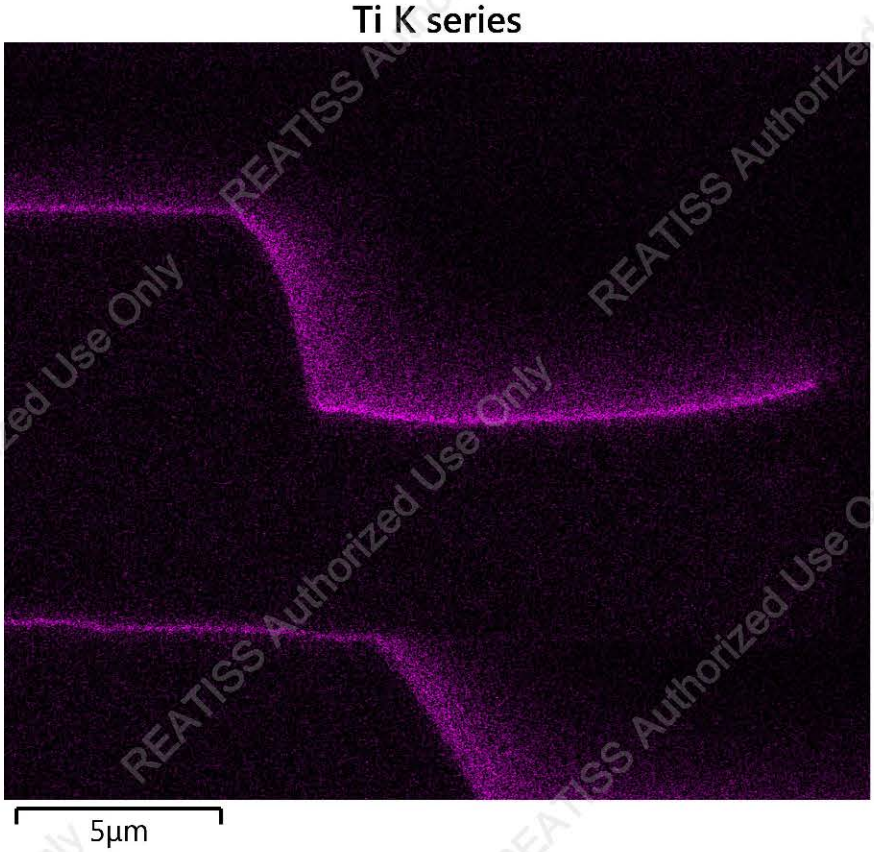

Figure 68. Titanium EDX map layer

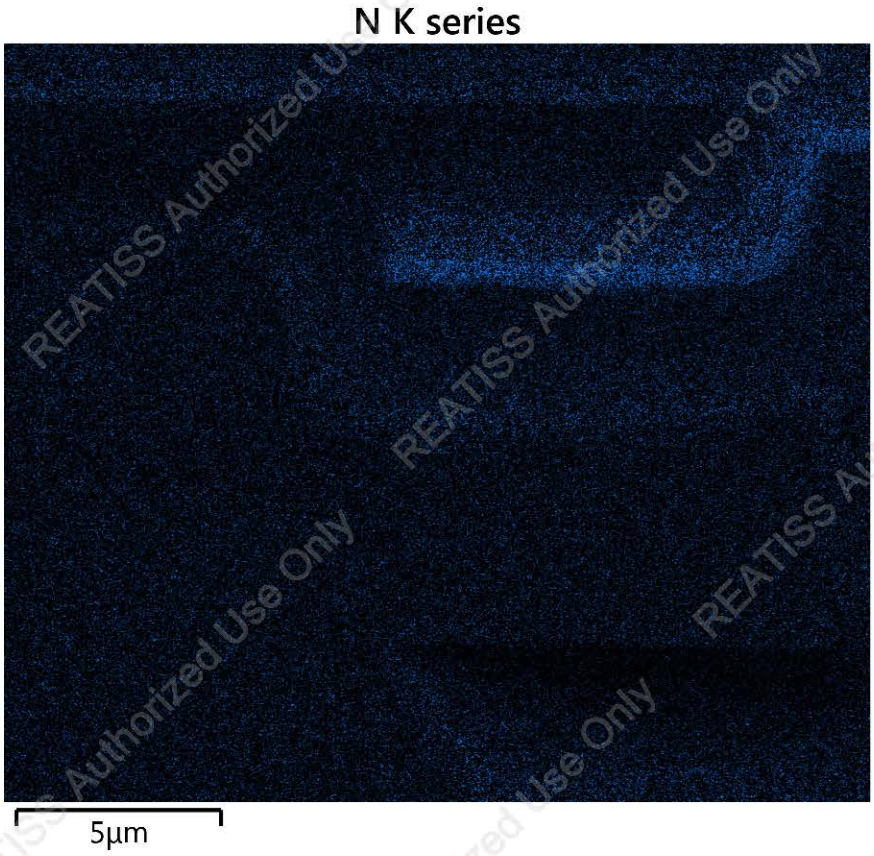

Figure 69. Nitrogen EDX map layer

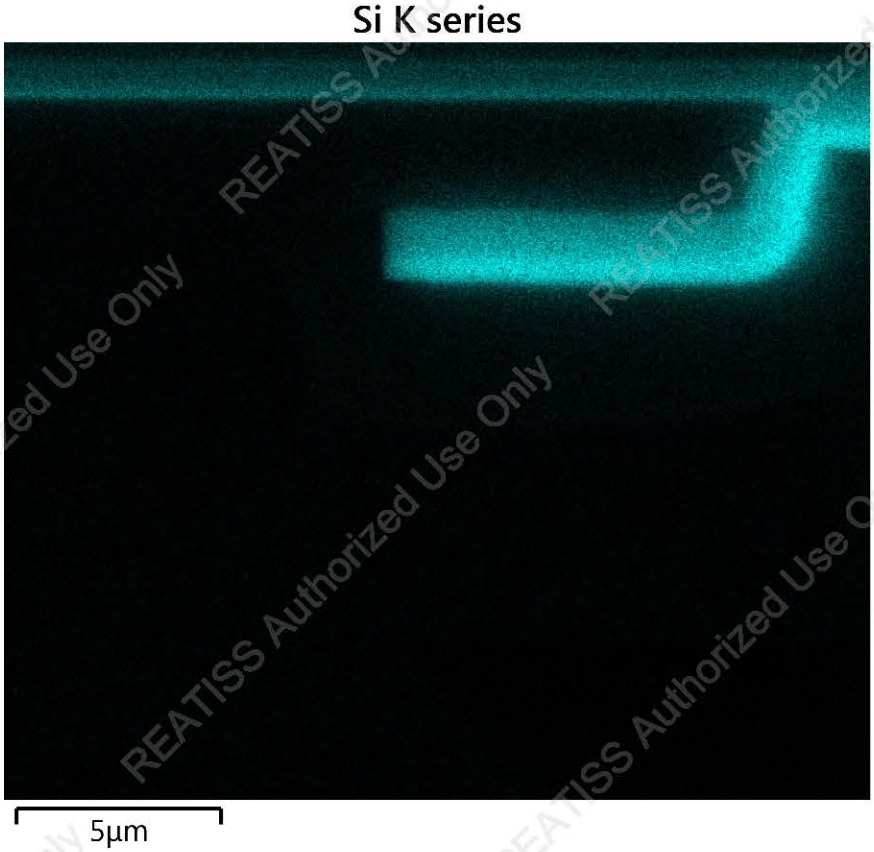

Figure 70. Silicon EDX map layer

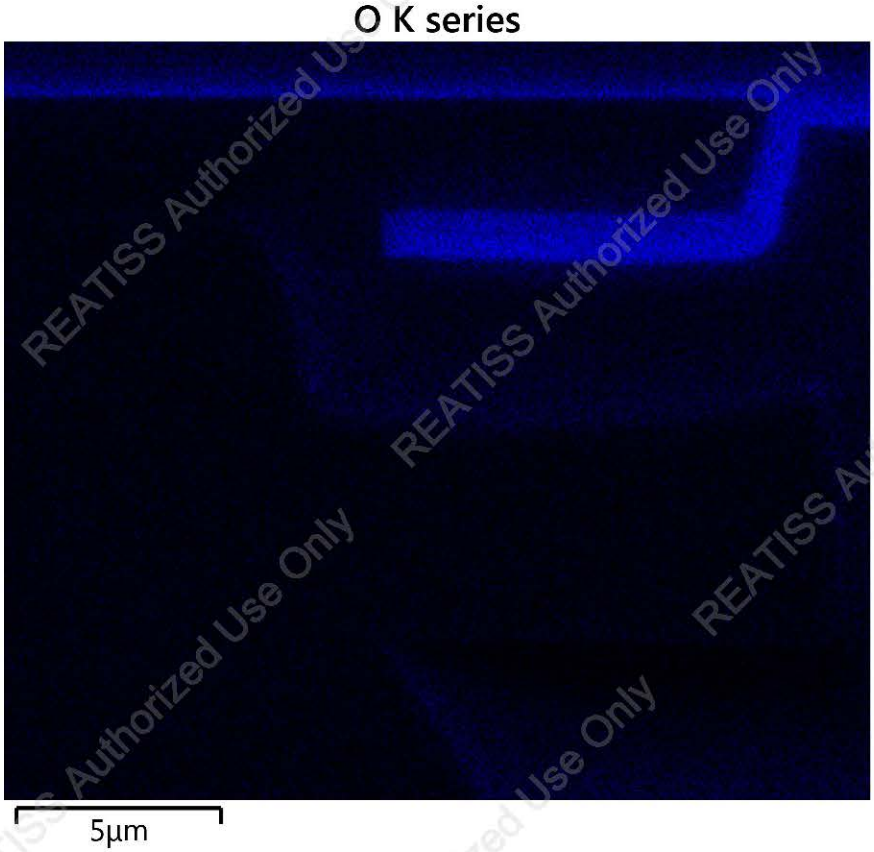

Figure 71. Oxygen EDX map layer

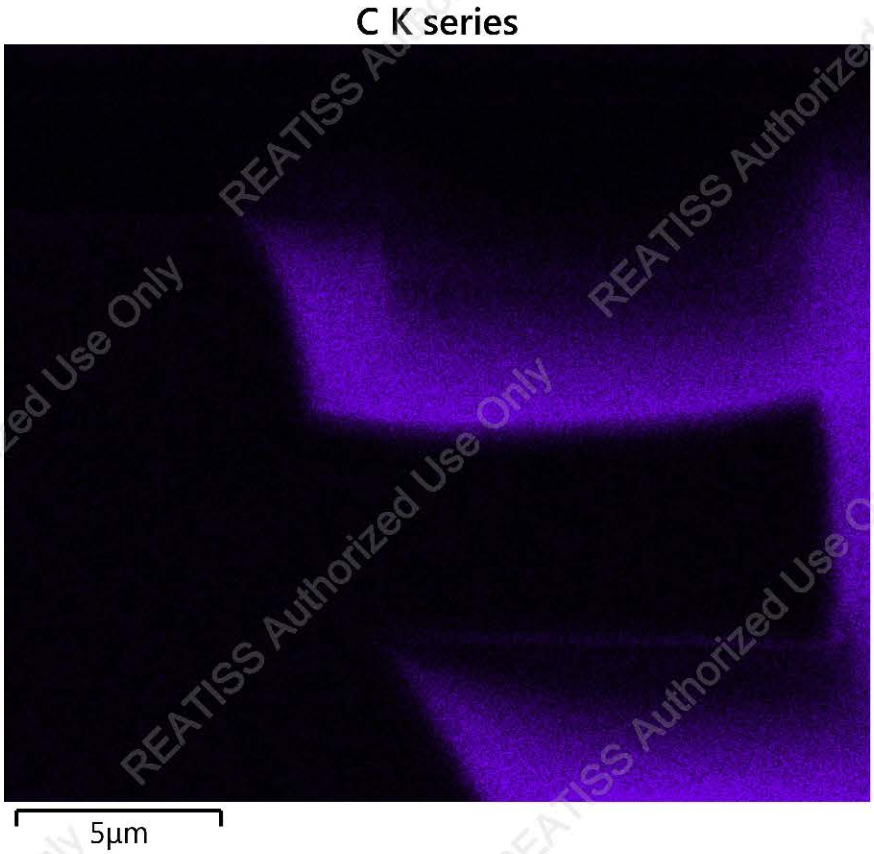

Figure 72. Carbon EDX map layer

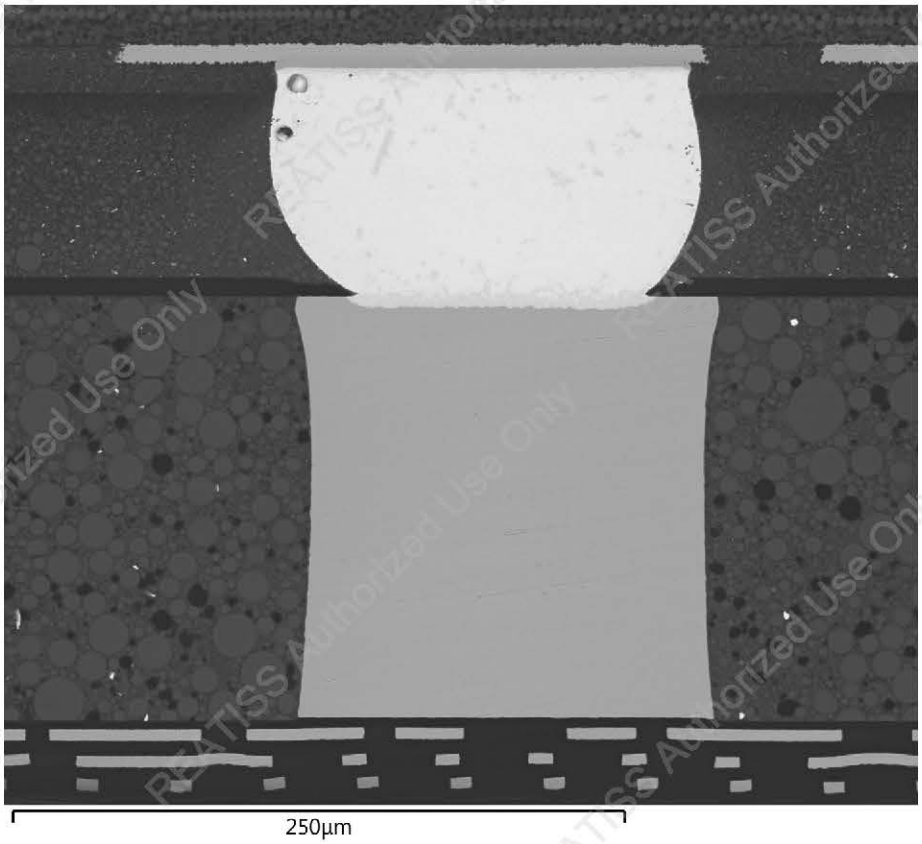

Figure 73. Package connection solder ball and TMV

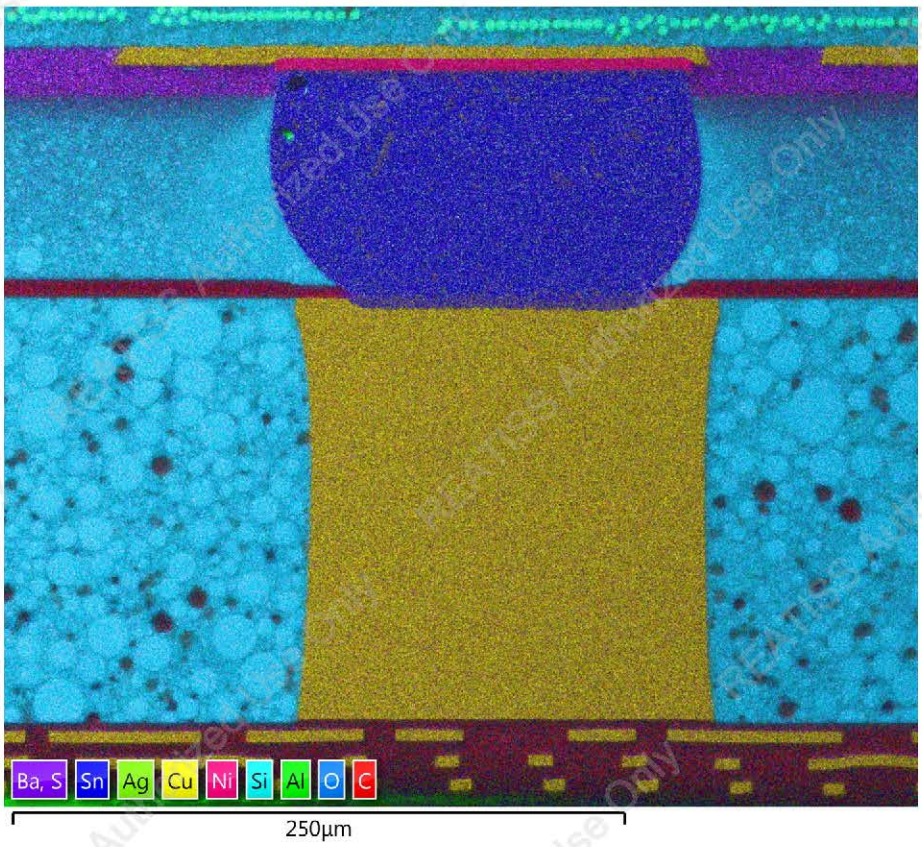

Figure 74. Layered EDX map of package connection solder ball and TMV

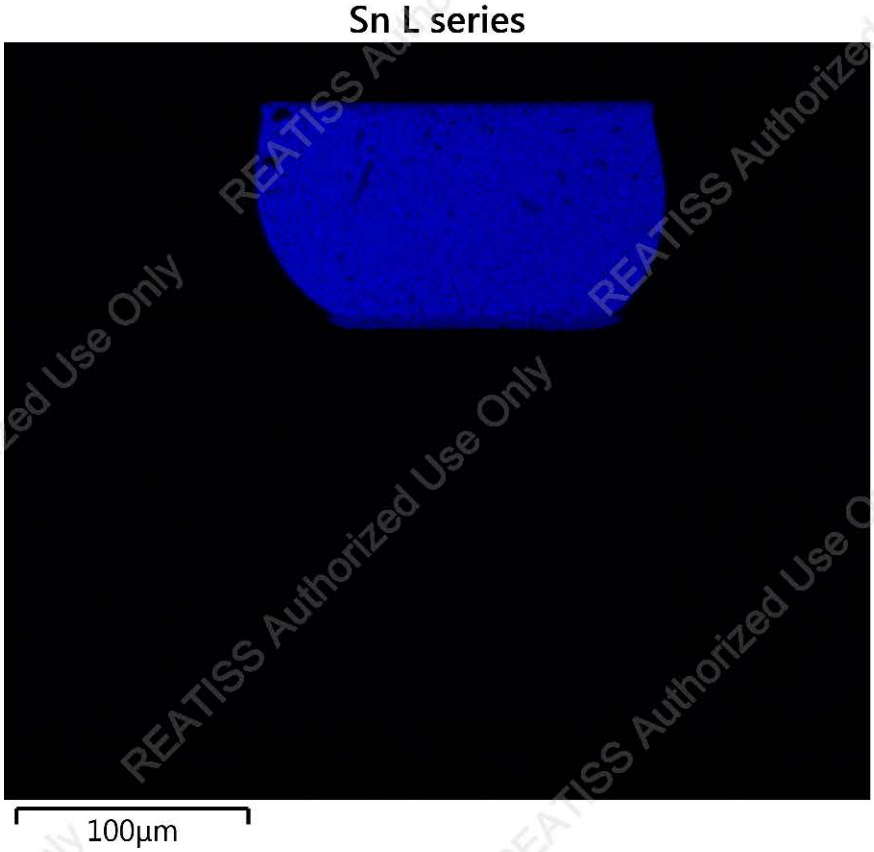

Figure 75. Tin EDX map layer

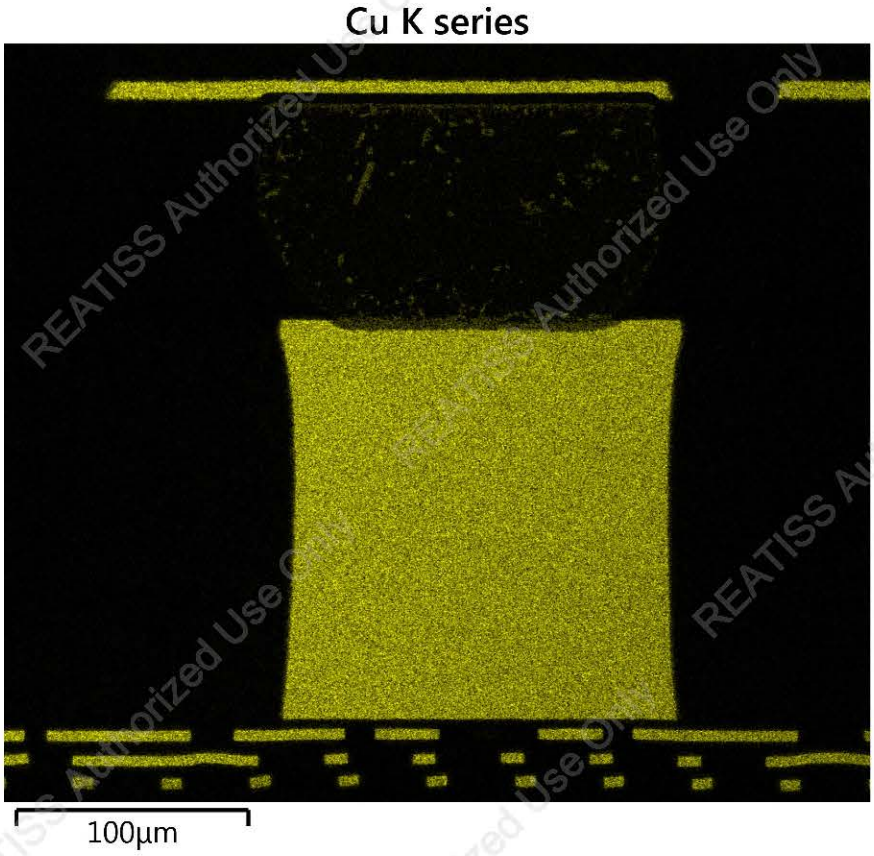

Figure 76. Copper EDX map layer

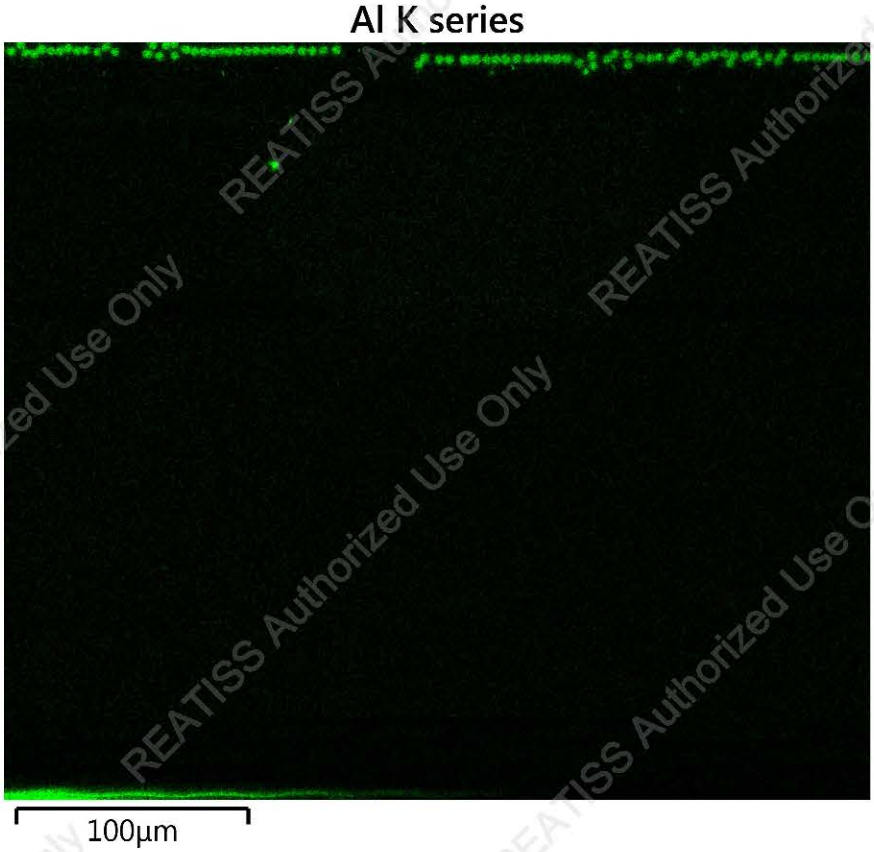

Figure 77. Aluminum EDX map layer

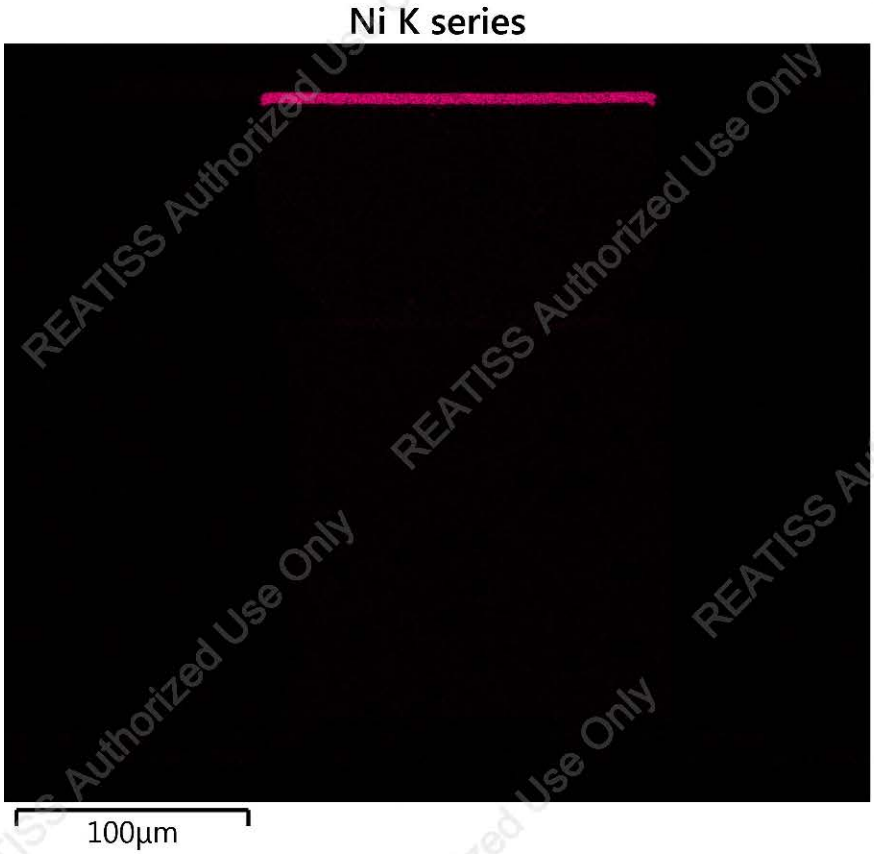

Figure 78. Nickel EDX map layer

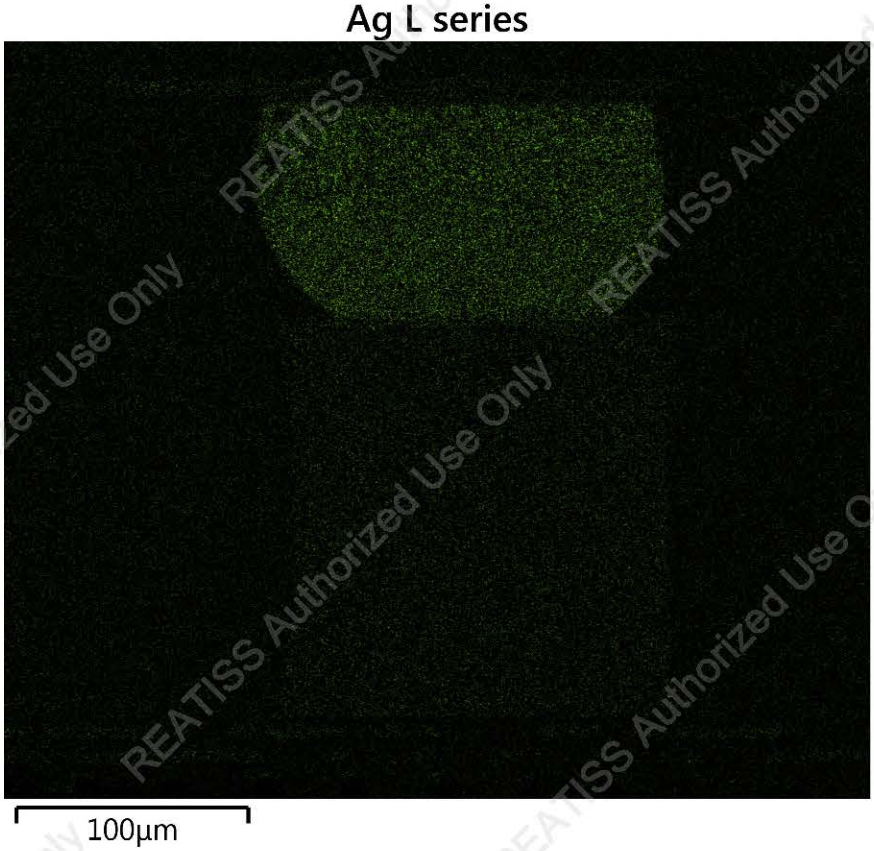

Figure 79. Silver EDX map layer

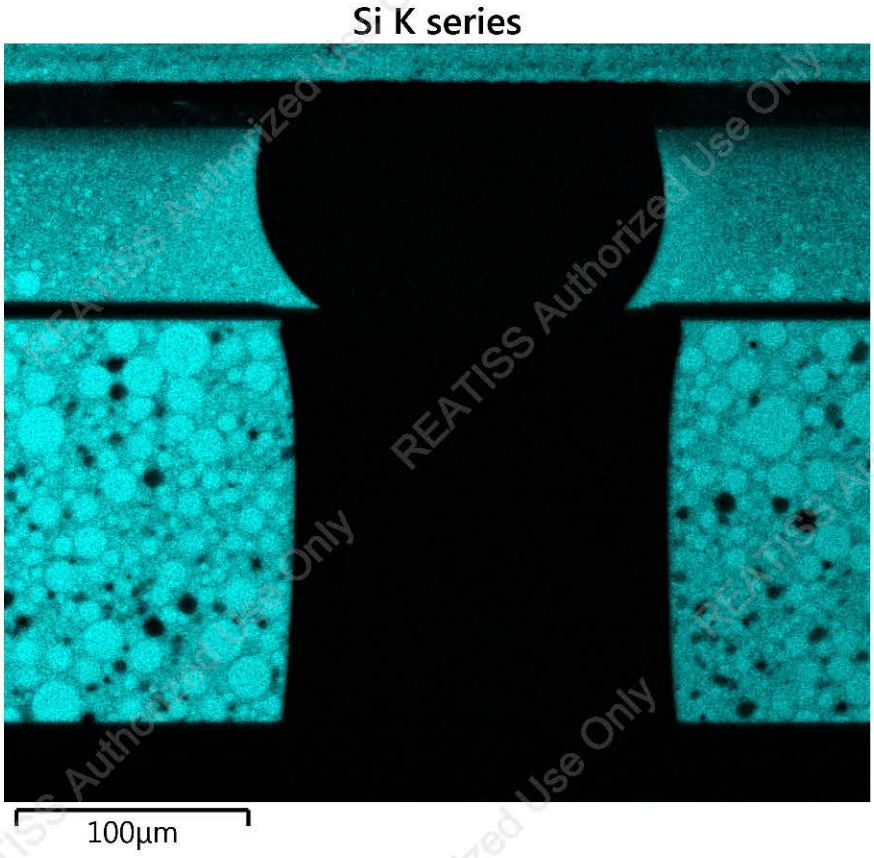

Figure 80. Silicon EDX map layer

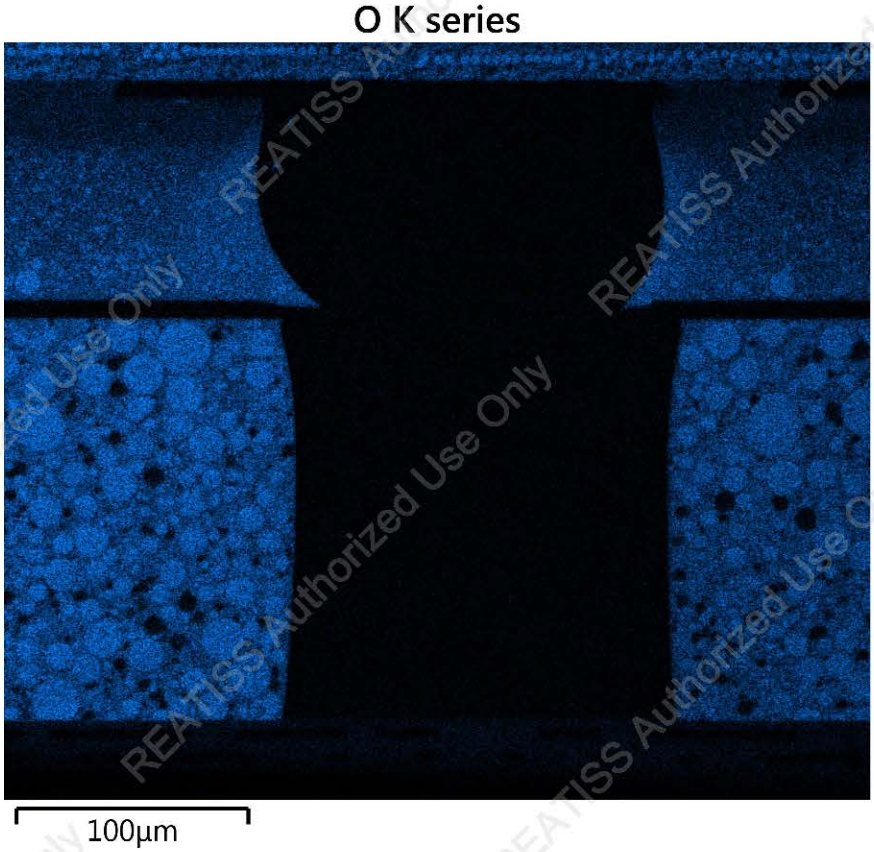

Figure 81. Oxygen EDX map layer

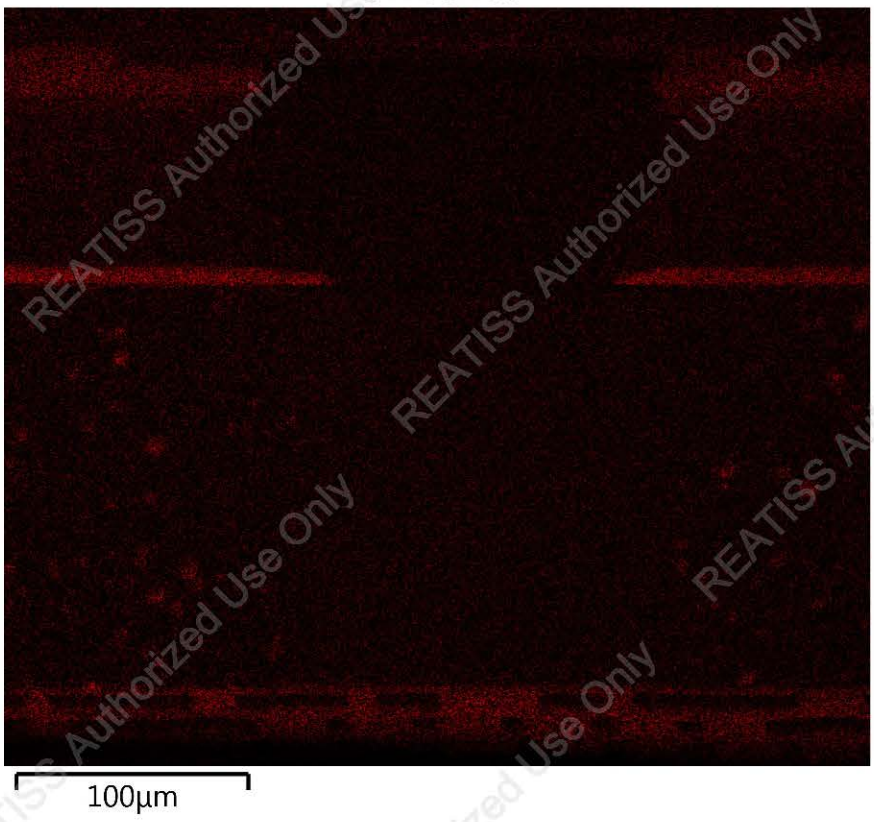

Figure 82. Carbon EDX map layer

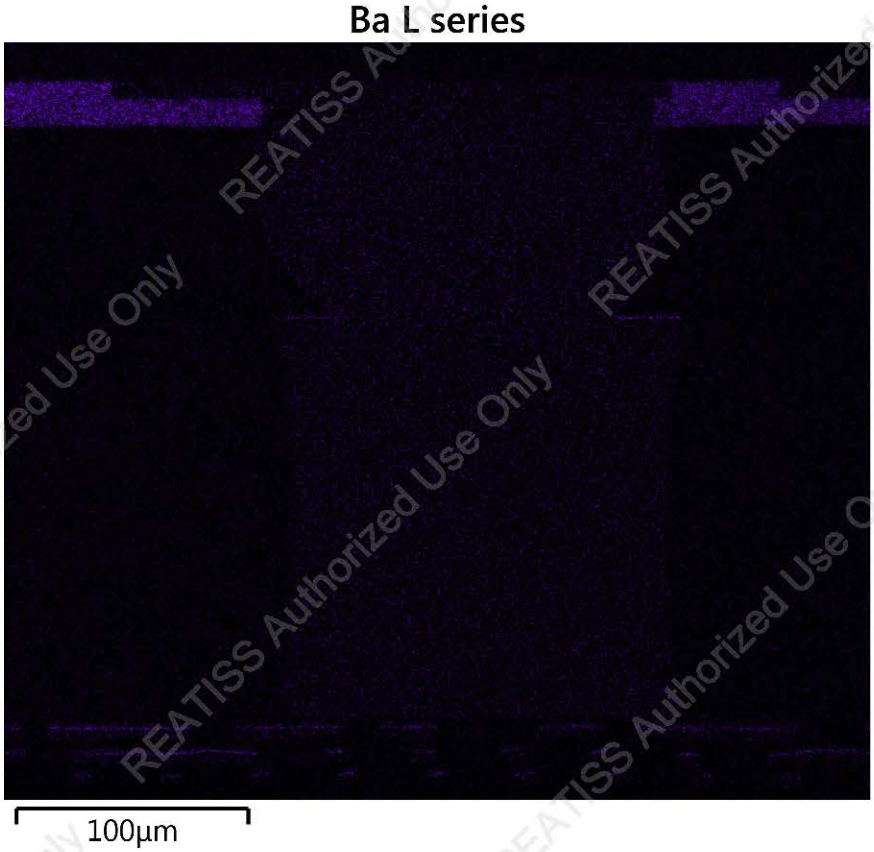

Figure 83. Barium EDX map layer

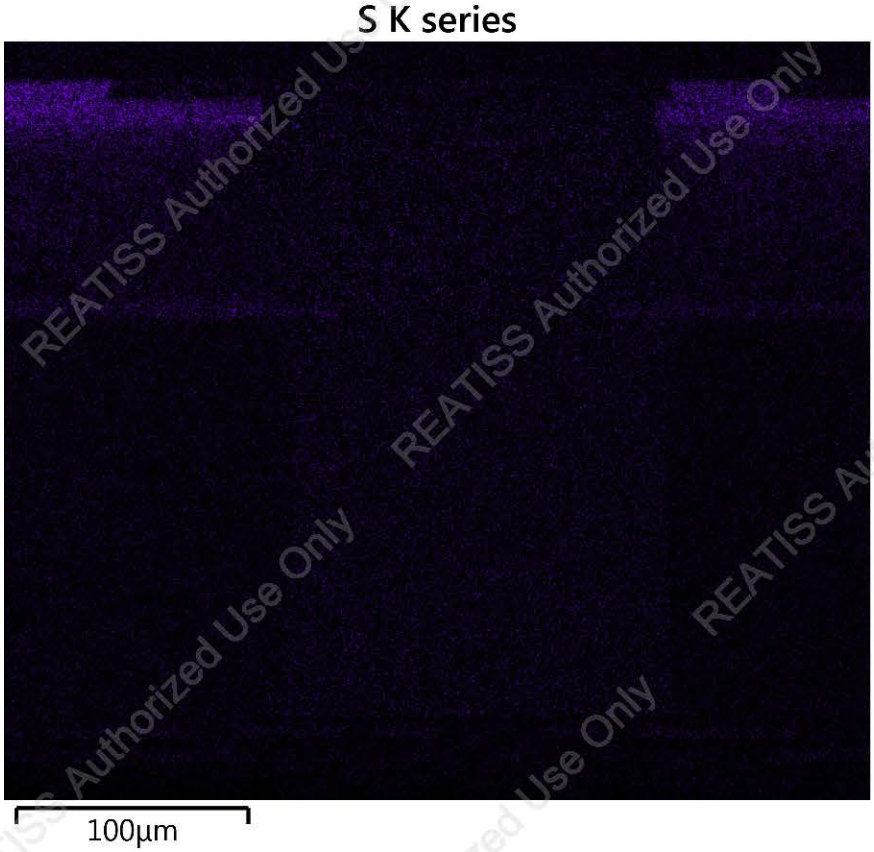

Figure 84. Sulfur EDX map layer

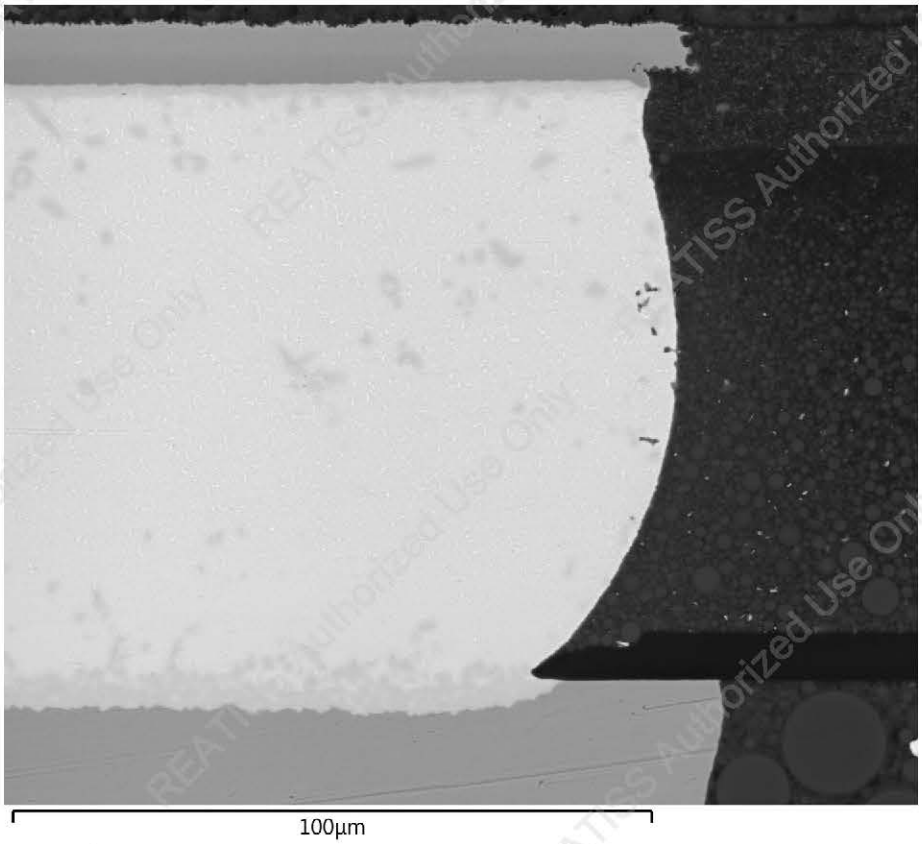

Figure 85. Package connection solder ball edge

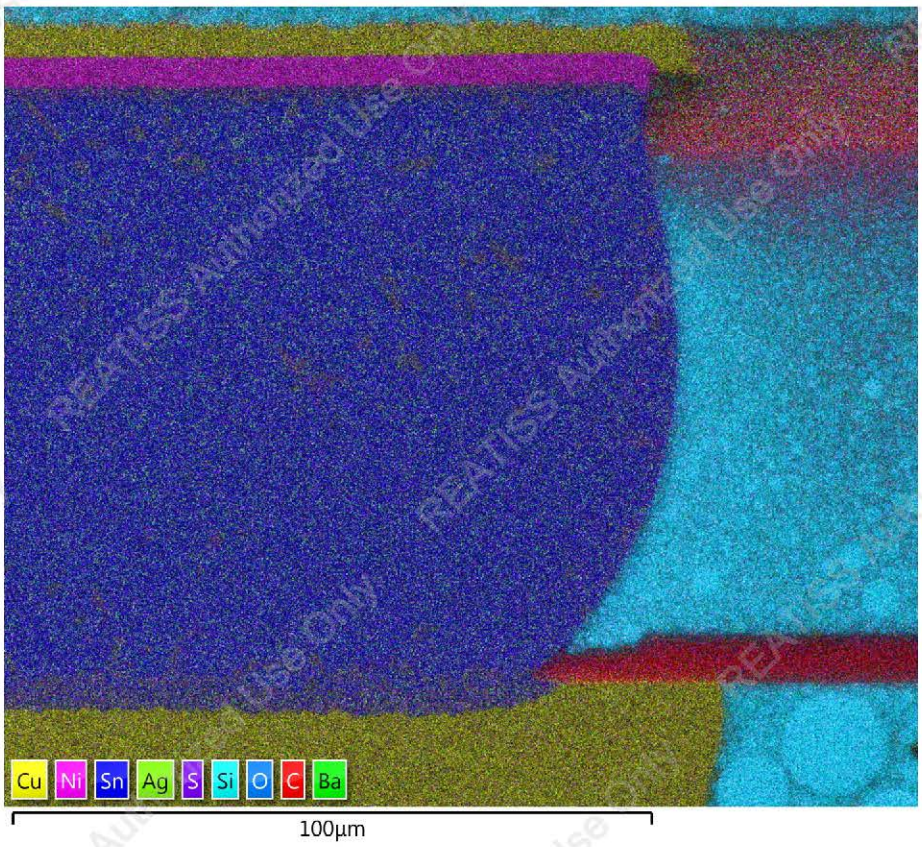

Figure 86. Layered EDX map of package connection solder ball edge

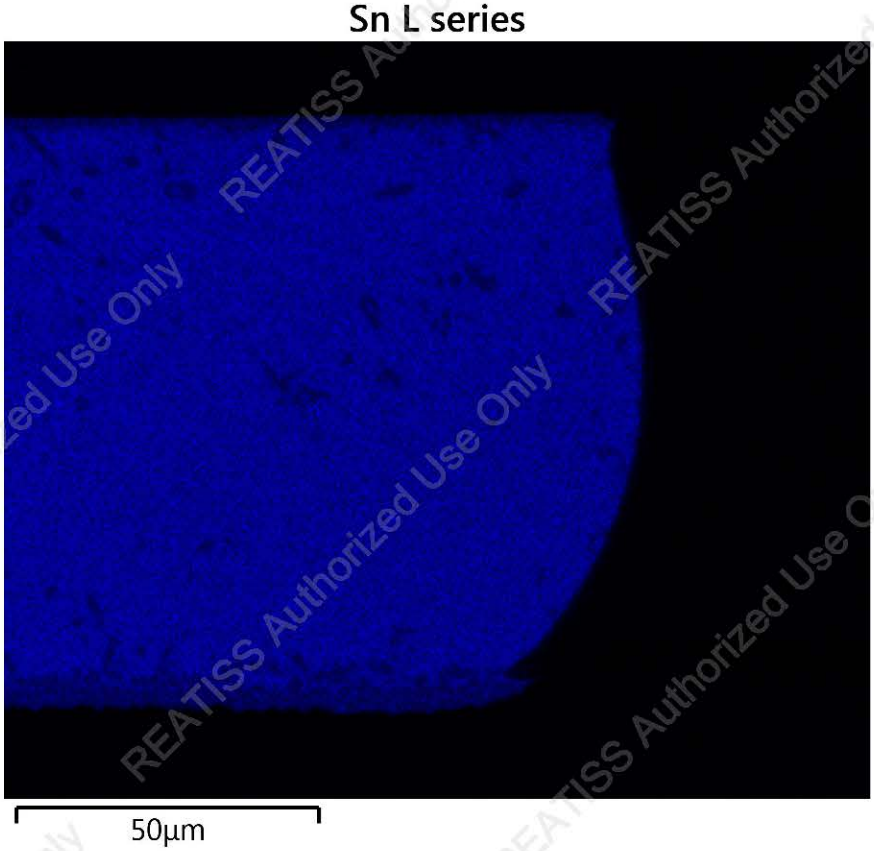

Figure 87. Tin EDX map layer

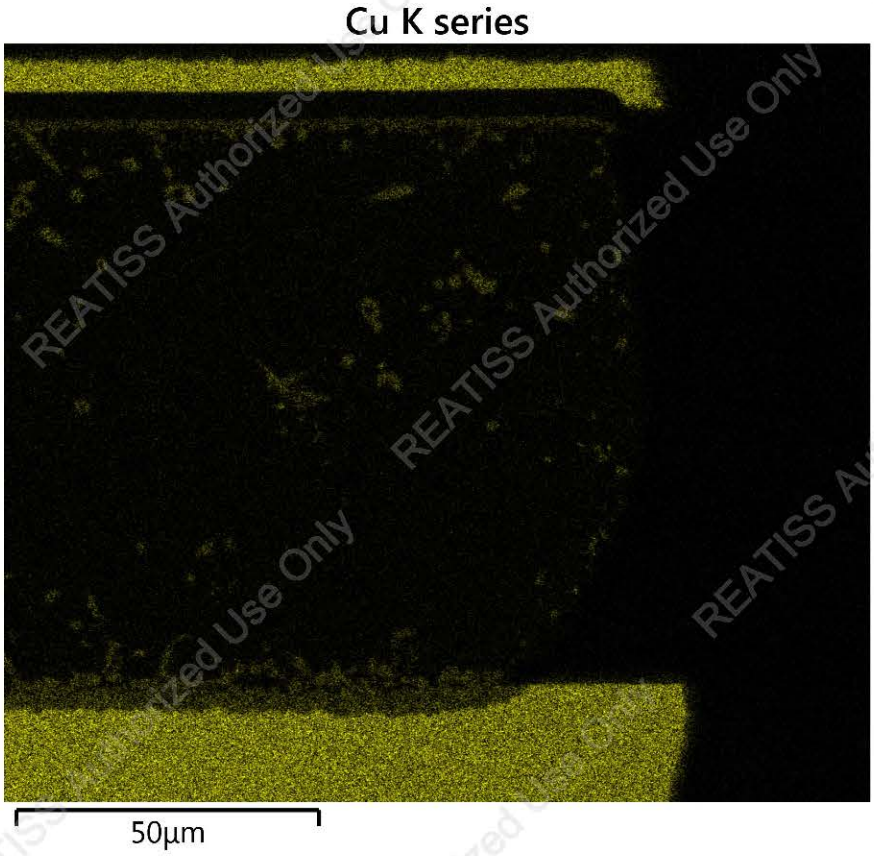

Figure 88. Copper EDX map layer

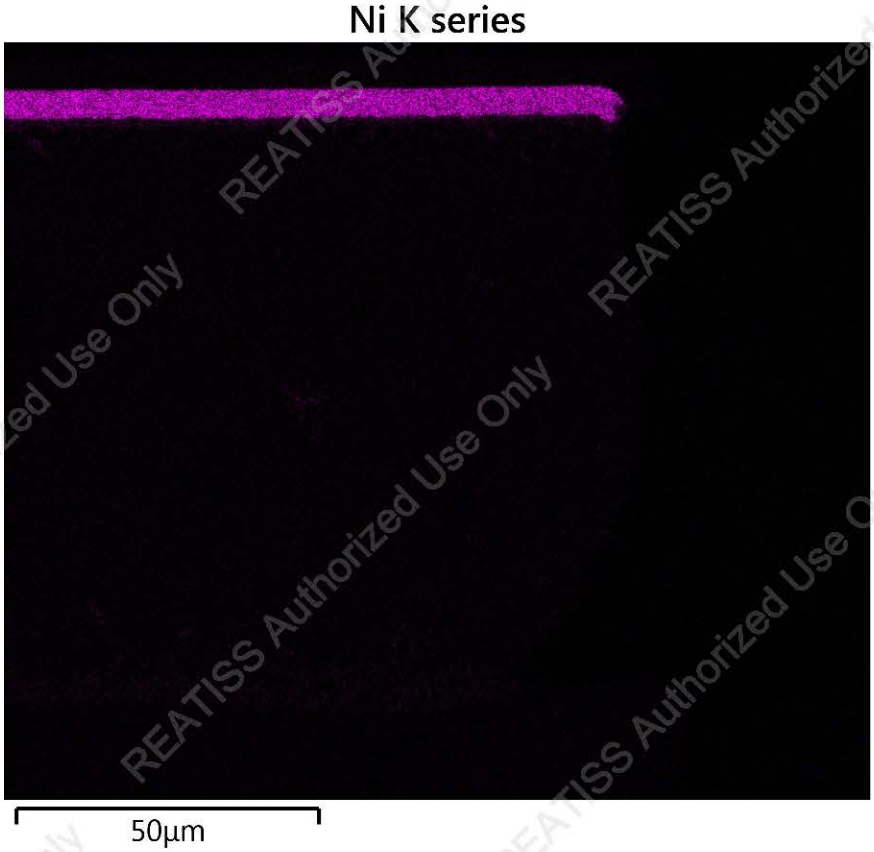

Figure 89. Nickel EDX map layer

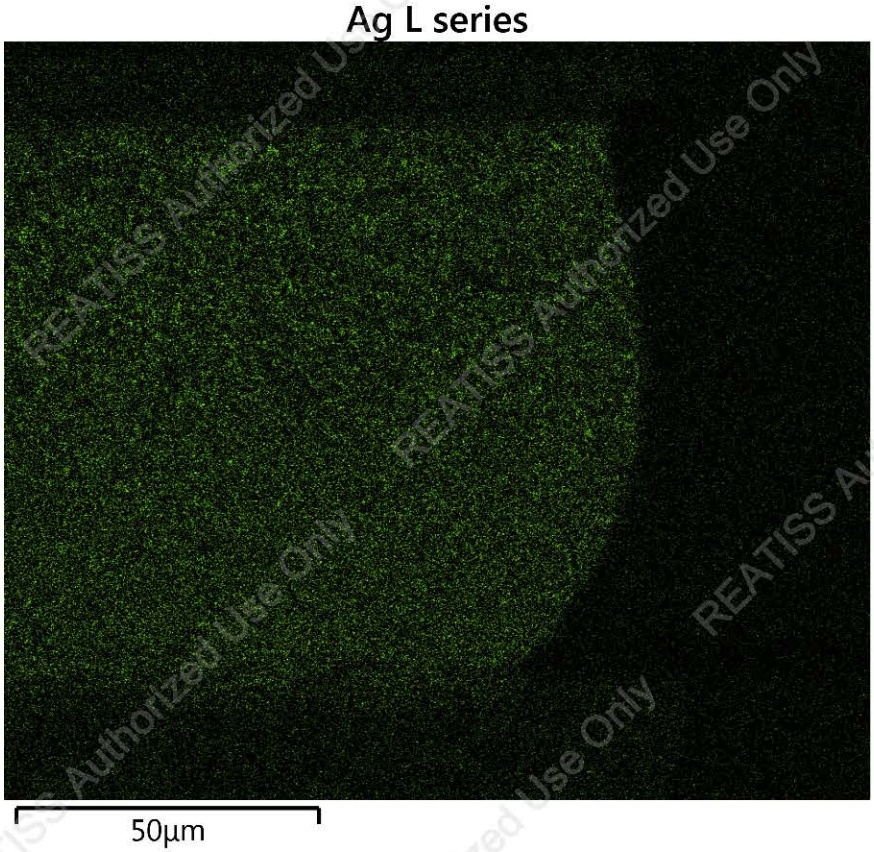

Figure 90. Silver EDX map layer

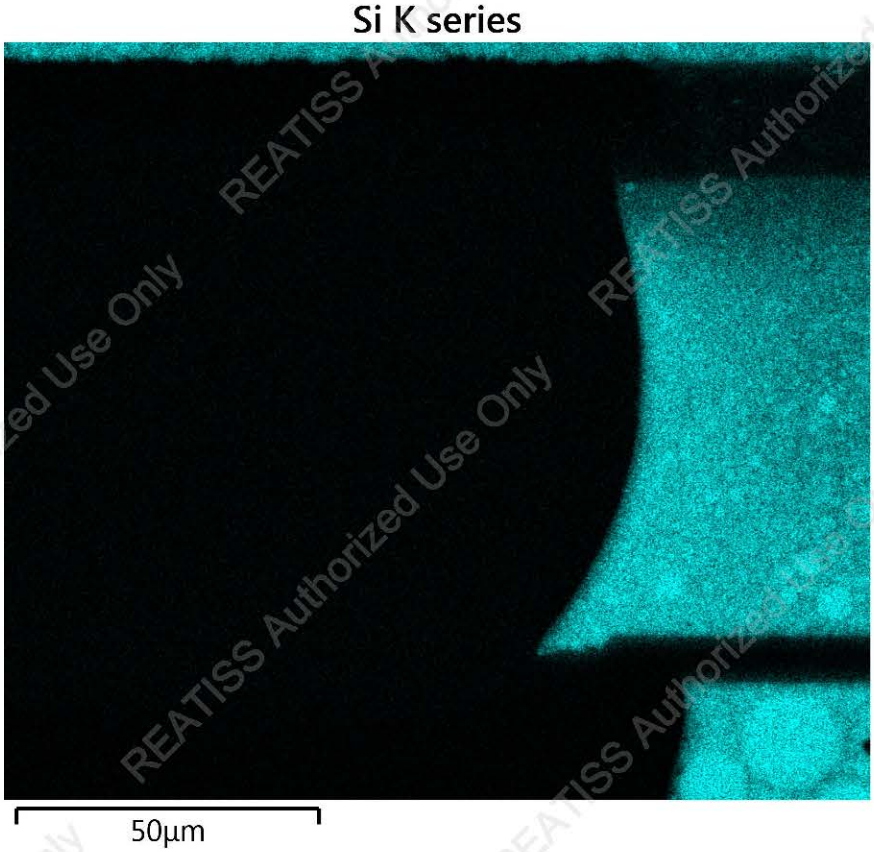

Figure 91. Silicon EDX map layer

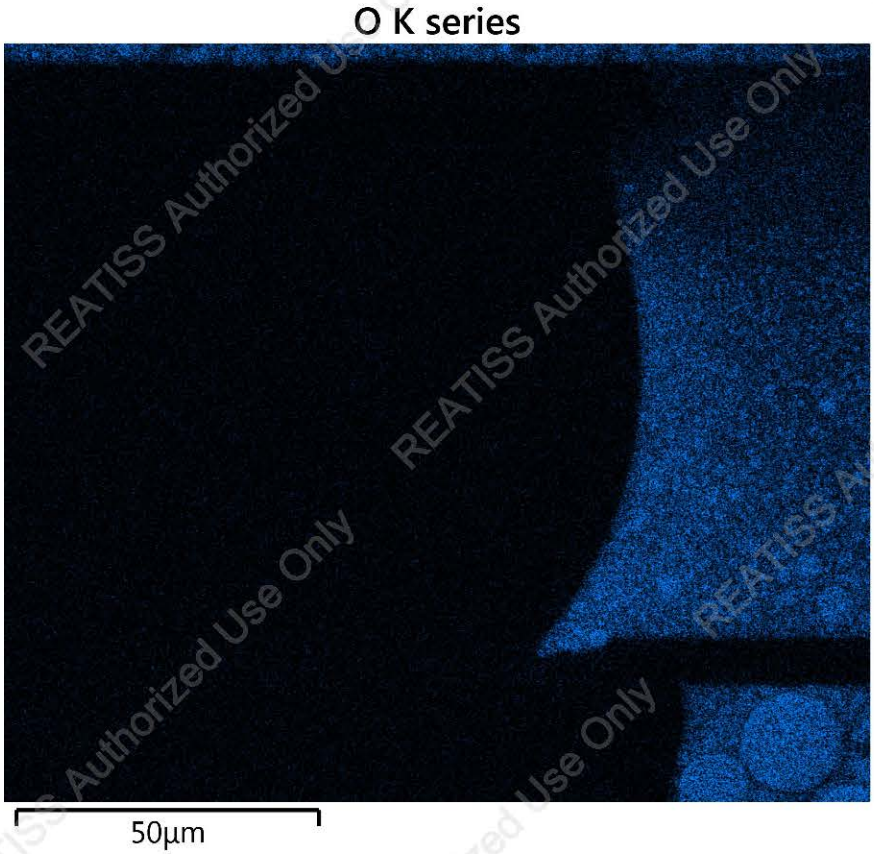

Figure 92. Oxygen EDX map layer

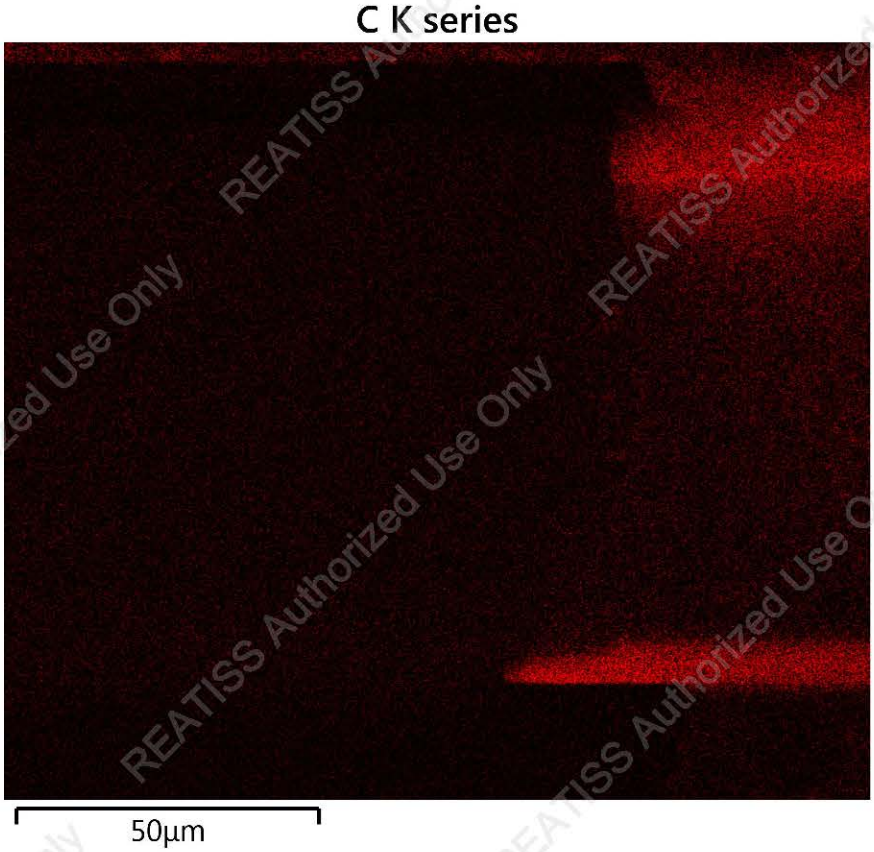

Figure 93. Carbon EDX map layer

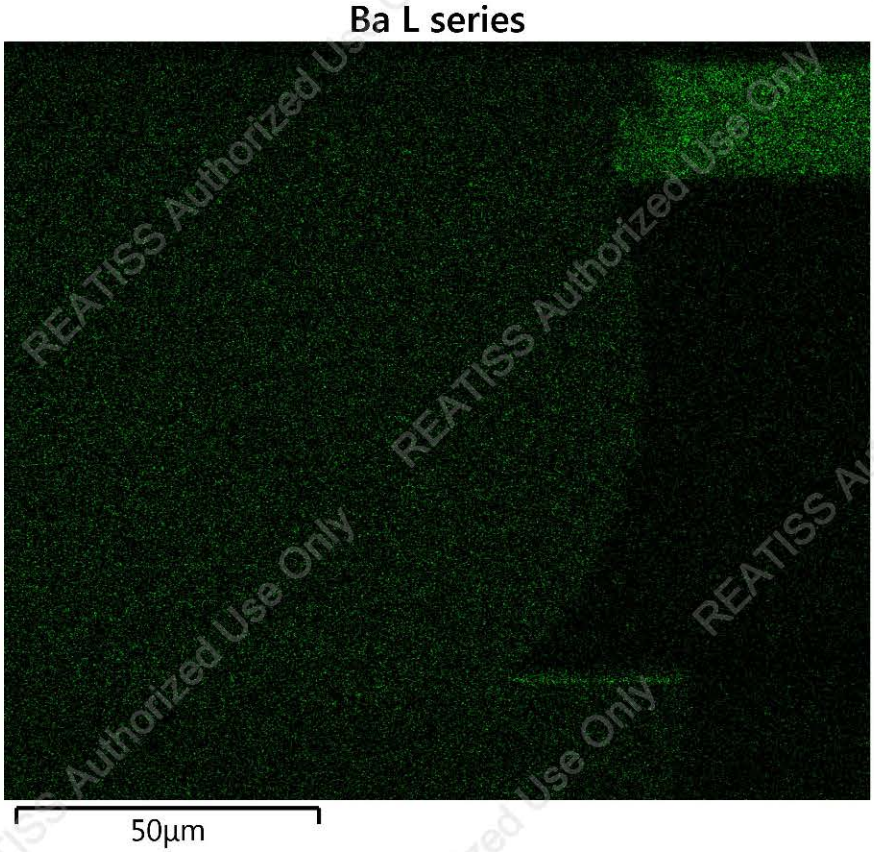

Figure 94. Barium EDX map layer

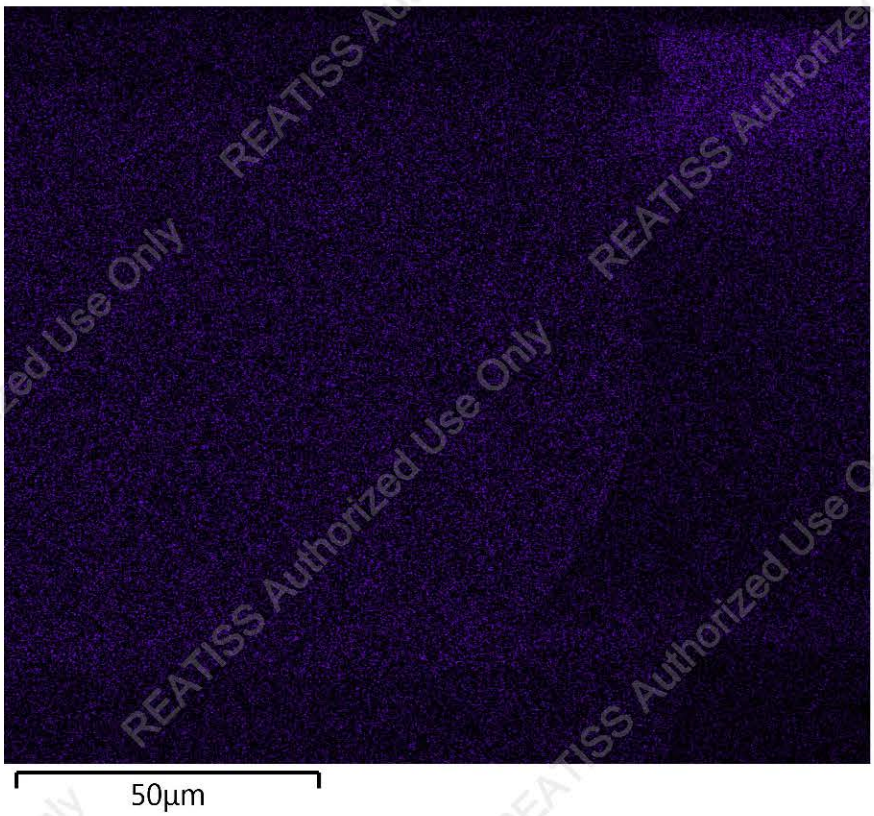

Figure 95. Sulfur EDX map layer